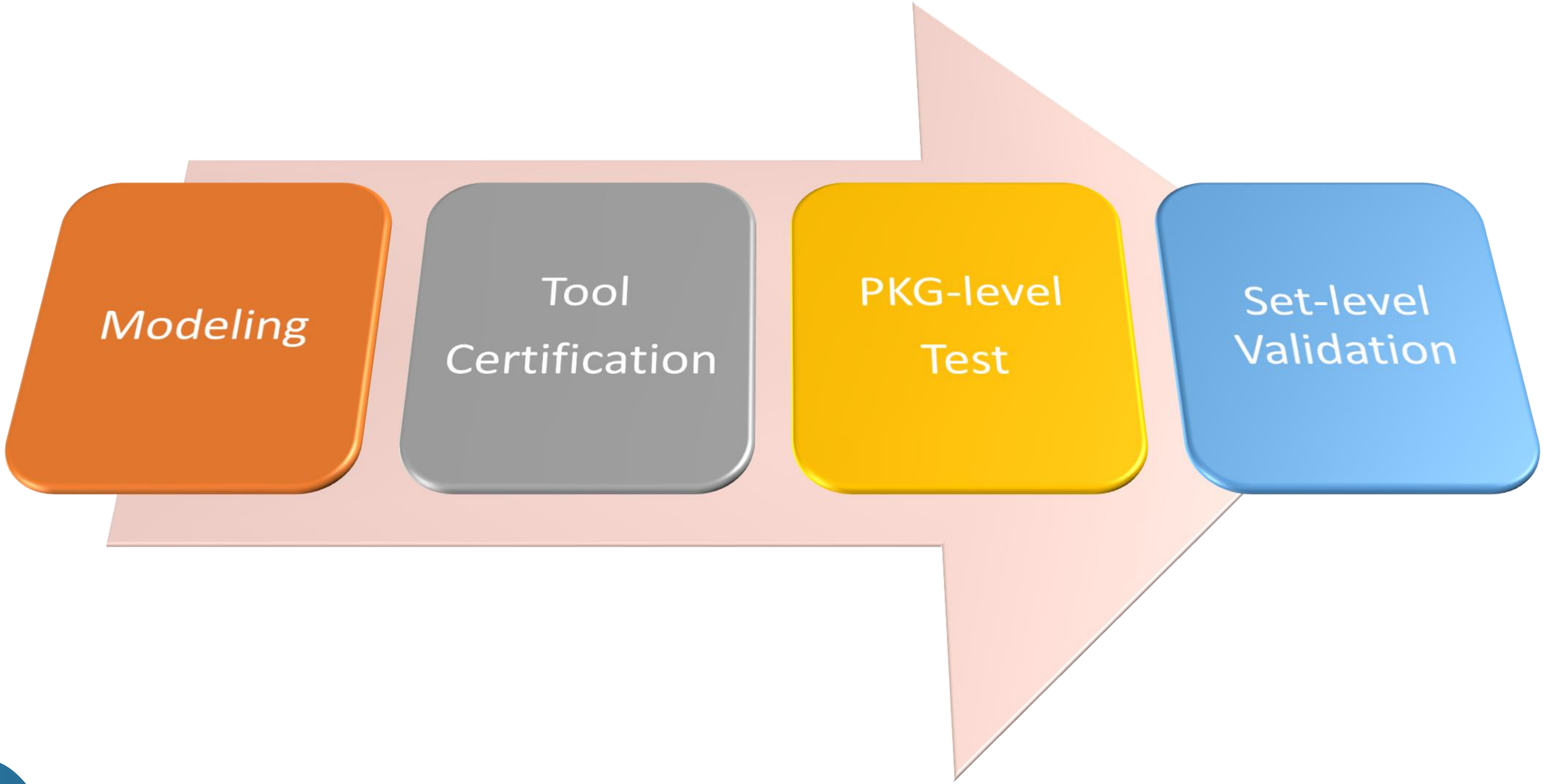
Thermal Management Studies in Samsung Electronics Corporation

Ki Wook Jung, Ph.D.

Contents of Today's Talk



Modeling

Tool Certification

PKG-level Test

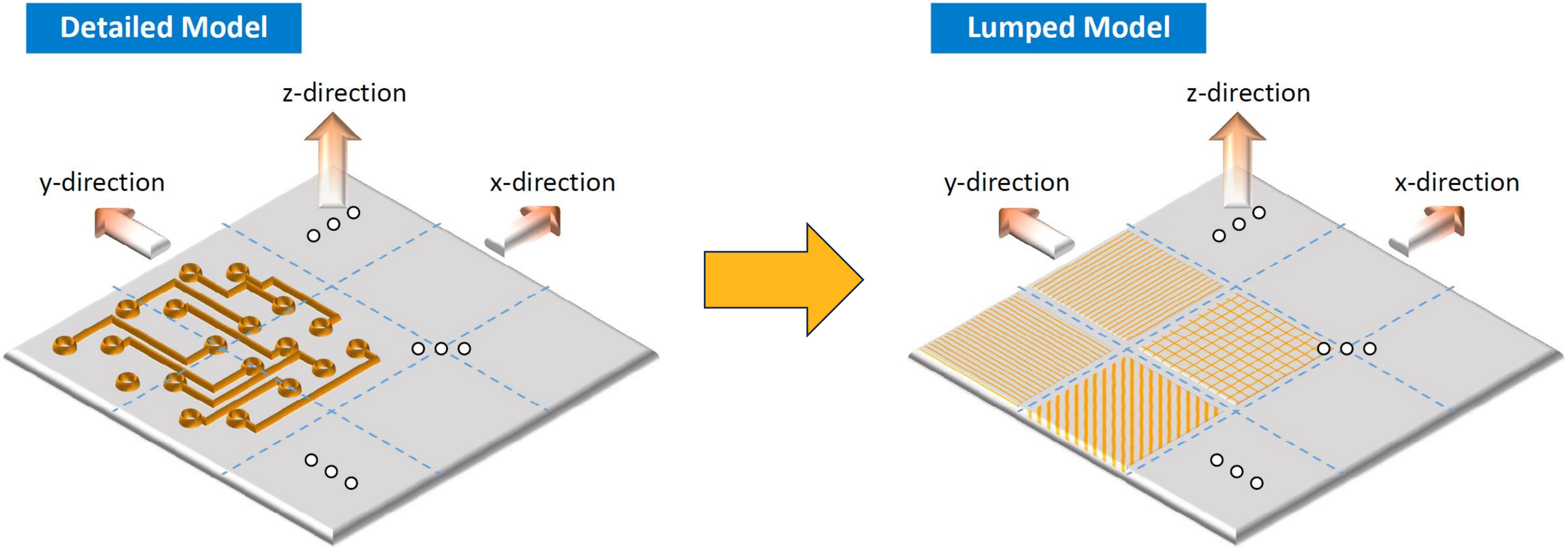
Set-level Validation

Modeling Methodology for ETC

** Effective Thermal Conductivity*

Modeling

Pursuit of simplicity and accuracy in on-chip/off-chip thermal simulation



Ref1: 10.1109/ECTC51909.2023.00041

Modeling Methodology for ETC

** Effective Thermal Conductivity*

Modeling

A general flow to estimate ETCs of metal patterns

Define input parameters: five structural factors

↓

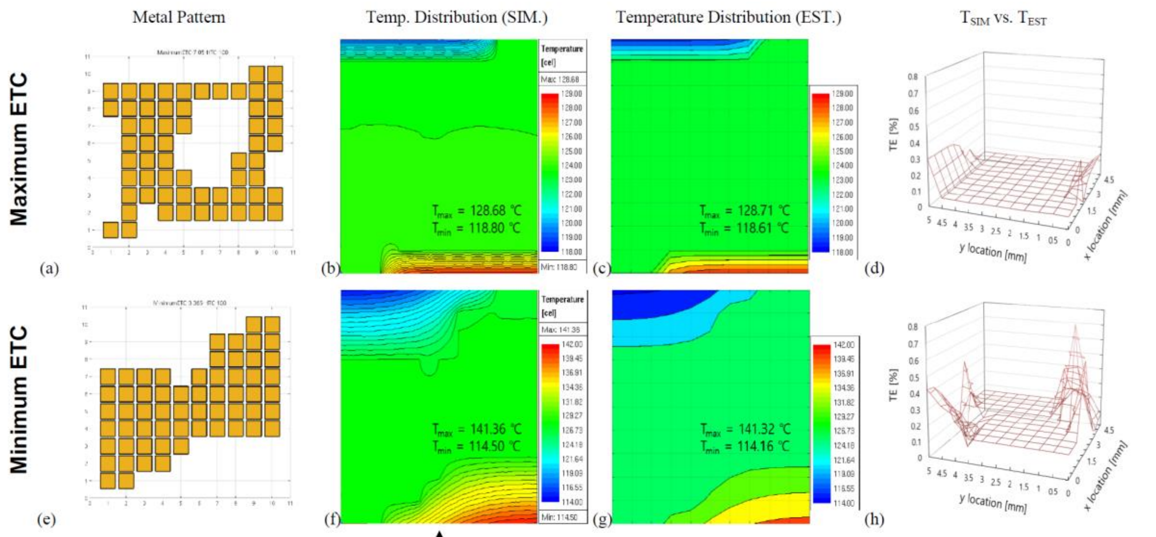
Generate metal patterns with one varying structural factor & varied HTC ← **Module 1:** Case Generator

↓

Calculate temperature at every vertex of a pixel and estimate ETCs of the defined metal patterns ← **Module 2: ETC Estimator**

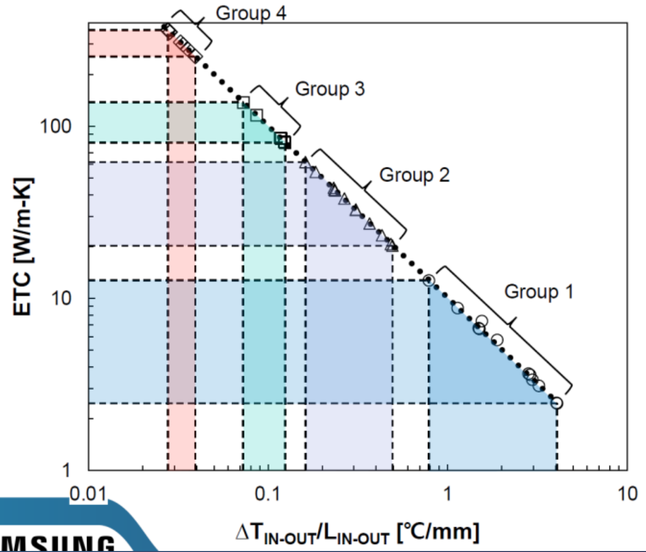
↓

Analyze the effect of individual input parameters on the calculated ETCs



↑ AEDT Icepak (2022R2)

Structural Parameters	Values
Metal Volume Fraction [%]	60
Inlet & Outlet Location [Pixel]	In: (1,1) Out: (9,10)
Inlet & Outlet Width [Pixel]	In: 2 Out: 2
Inlet & Outlet Width Ratio	1
Pixel Length [um]	500
Runtime/case	
SIM	**EST**
3.5 – 5 min	**0.4 – 6.1 sec**

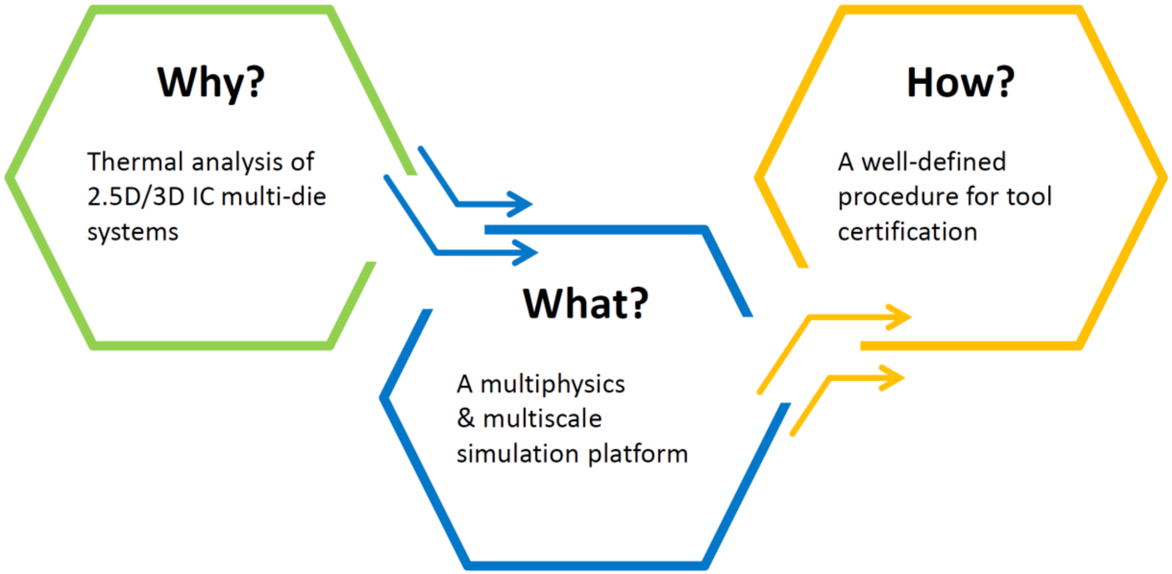


Structural Parameters	Group 1	Group 2	Group 3	Group 4
Metal Volume Fraction [%]	40	40	97	95
Inlet & Outlet Location [Pixel]	In: (1,1) Out: (9,10)	In: (1,1) Out: (2,10)	In: (1,1) Out: (2,10)	In: (1,1) Out: (1,10)
Inlet & Outlet Width [Pixel]	In: 2 Out: 2	In: 9 Out: 9	In: 9 Out: 9	In: 10 Out: 10
Inlet & Outlet Width Ratio	1	1	1	1
Pixel Length [um]	5	5	5	5
ETC range [W/m-K]	2.45E0 – 1.27E1	2.07E1 – 6.20E1	8.04E1 – 1.38E2	2.54E2 – 3.62E2
$\Delta T_{IN\text{-}OUT}/L_{IN\text{-}OUT}$ range [°C/mm]	4.08E0 – 7.86E-1	4.83E-1 – 1.61E-1	1.24E-1 – 7.28E-2	3.93E-2 – 2.76E-2

Ref1: 10.1109/ECTC51909.2023.00041

Certifying a Thermal Analysis Tool

Three key questions to be answered today



Why?
Thermal analysis of 2.5D/3D IC multi-die systems

What?
A multiphysics & multiscale simulation platform

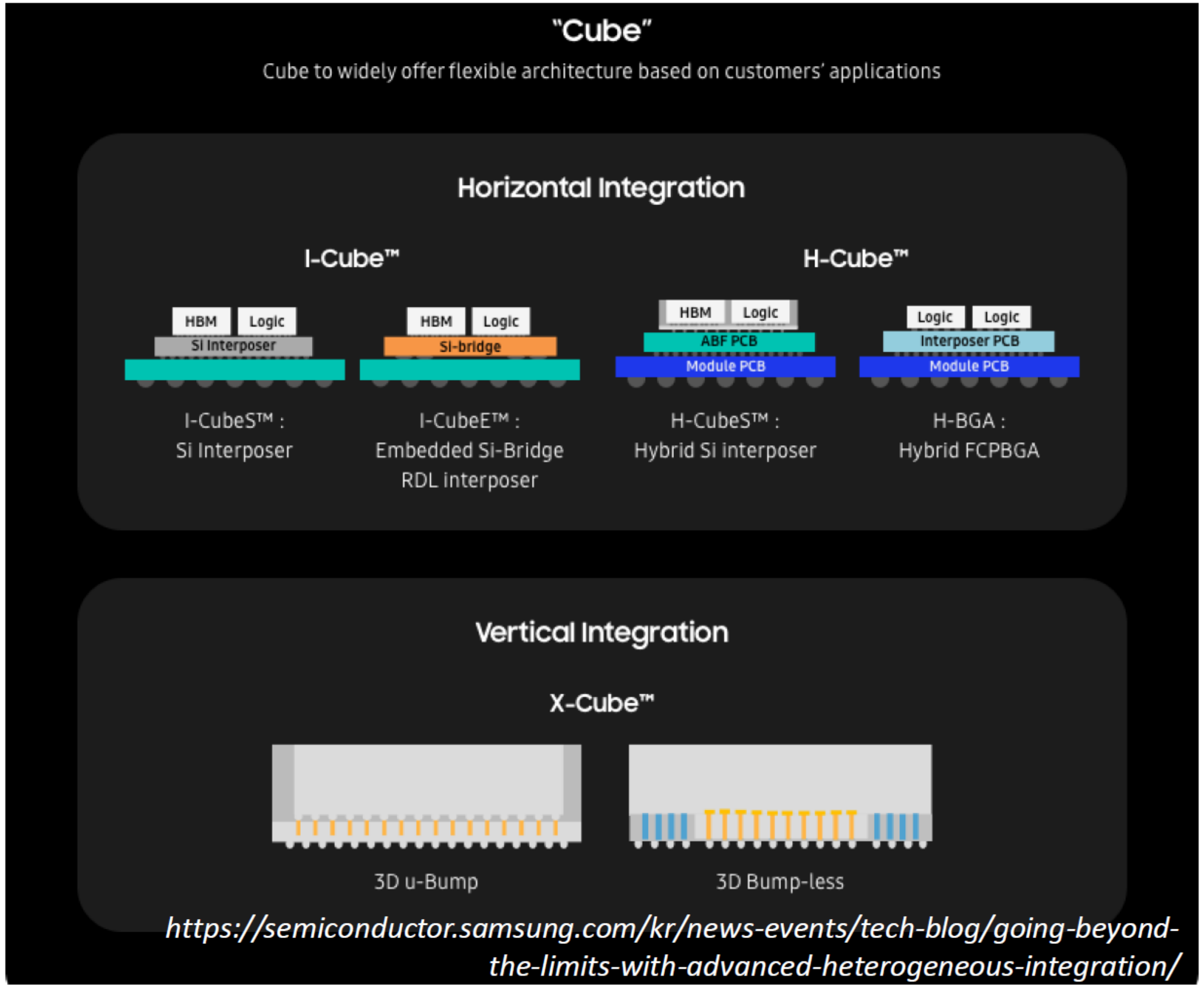
How?
A well-defined procedure for tool certification

Icepak

VS.

RedHawk-SC Electrothermal

Samsung Foundry's Advanced Heterogeneous Integration *(@ SFF 2022)*



"Cube"

Cube to widely offer flexible architecture based on customers' applications

Horizontal Integration

I-Cube™

H-Cube™

I-CubeS™ : Si Interposer

I-CubeE™ : Embedded Si-Bridge RDL interposer

H-CubeS™ : Hybrid Si interposer

H-BGA : Hybrid FCPBGA

Vertical Integration

X-Cube™

3D u-Bump

3D Bump-less

https://semiconductor.samsung.com/kr/news-events/tech-blog/going-beyond-the-limits-with-advanced-heterogeneous-integration/

Certifying a Thermal Analysis Tool

Tool Certification

IEEE ELECTRONICS PACKAGING SOCIETY

ECTC
The 2024 IEEE 74th Electronic Components and Technology Conference

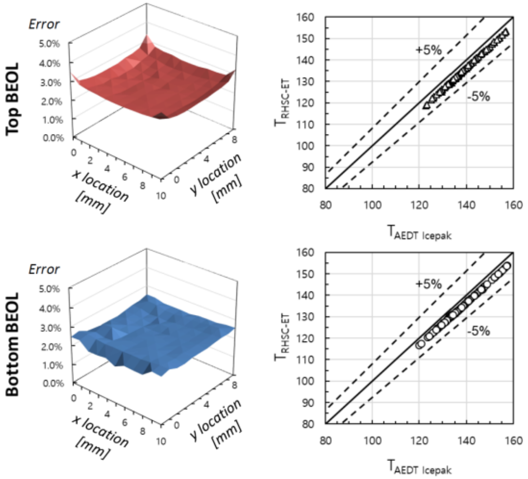
- ***Steady-state***

Metric	Criteria	Remarks
T_{max}, T_{min}	±5%	Max/min temp.
T_{pt1}, T_{pt2}, …	±5%	All monitor points' temp.

- ***Transient***

Metric	Criteria	Remarks
T_{max}, T_{min}	±10%	Max/min temp.
T_{pt1}, T_{pt2}, …	±10%	All monitor points' temp.
τ_{pt1}, τ_{pt2}, …	±10%	Thermal time constant

Steady-state summary



Top BEOL

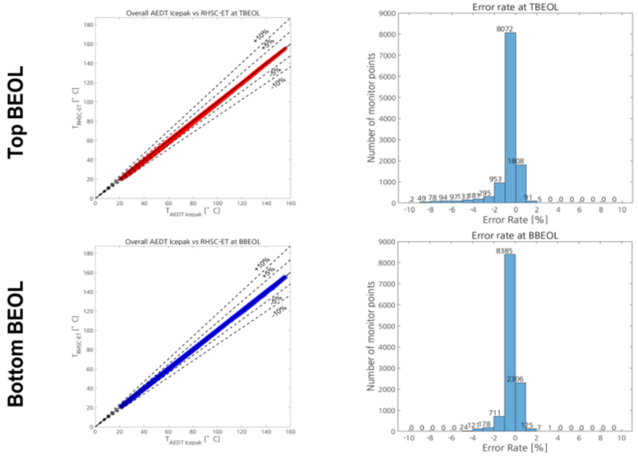
Diff. Rate	# of points
0-3%	116
3-5%	5
5-10%	0
> 10%	0
Total # of points	121

Bottom BEOL

Diff. Rate	# of points
0-3%	121
3-5%	0
5-10%	0
> 10%	0
Total # of points	121

**Error = $(T_{Icepak}-T_{RHSC-ET})/T_{Icepak}$*

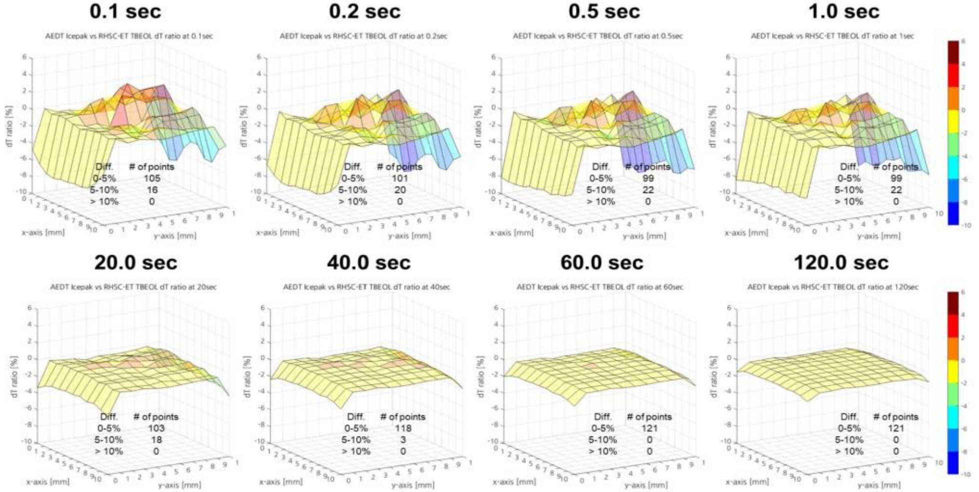
Transient summary



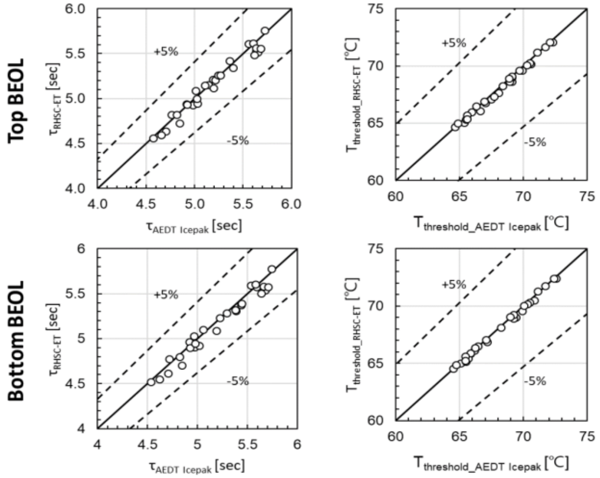
Diff. Rate	# of points
0-5%	11538
5-10%	320
> 10%	0
Total # of points	11858

Diff. Rate	# of points
0-5%	11858
5-10%	0
> 10%	0
Total # of points	11858

Error rate trend



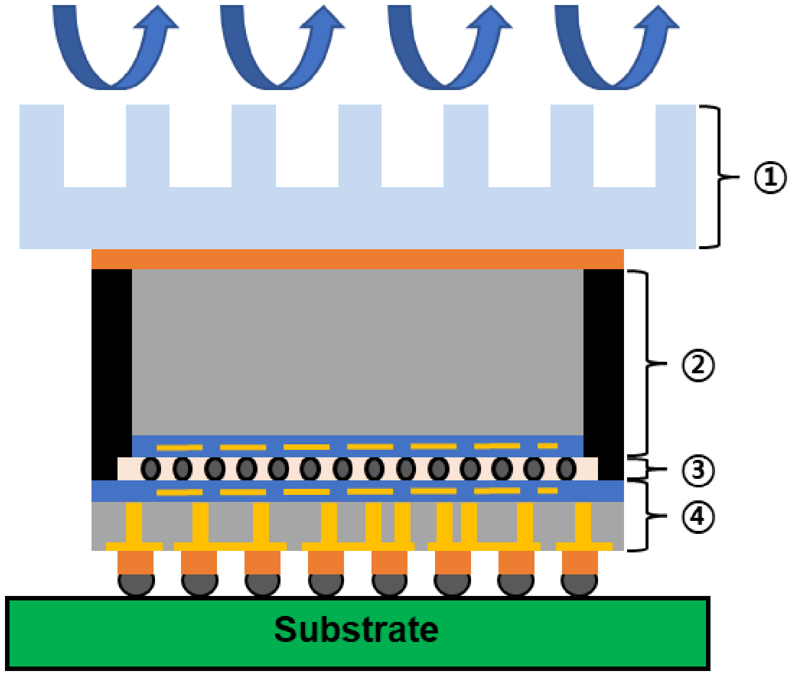
Thermal time constant

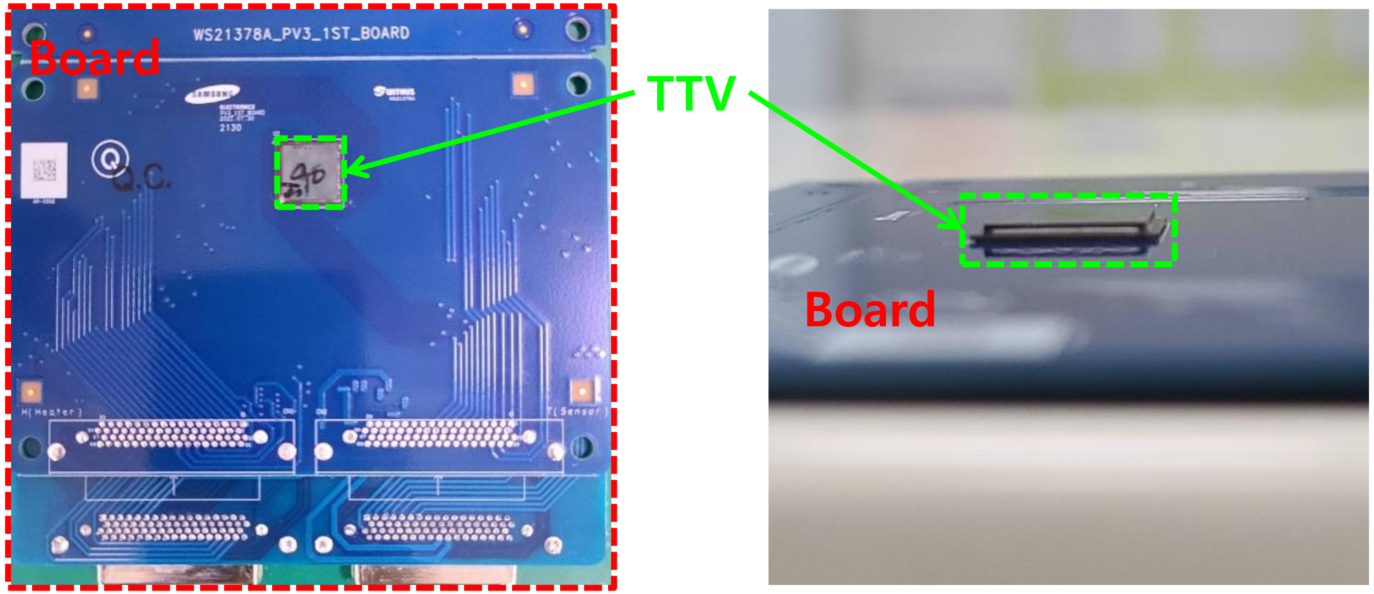


SAMSUNG & Ansys

PKG-level Thermal Management Tests

3DIC TTV Test setup





A heat sink with minichannels array (①) is used to dissipate heat from the 3D TTV to chilled coolant, DI water, at 25℃. Heaters and RTDs (— — —) are defined in Back-End-of-Lines (BEOLs, ■) of top/bottom chips (②,④). The joint-gap between top and bottom chips (③) consists of 50k microbumps and non-conductive film (NCF).

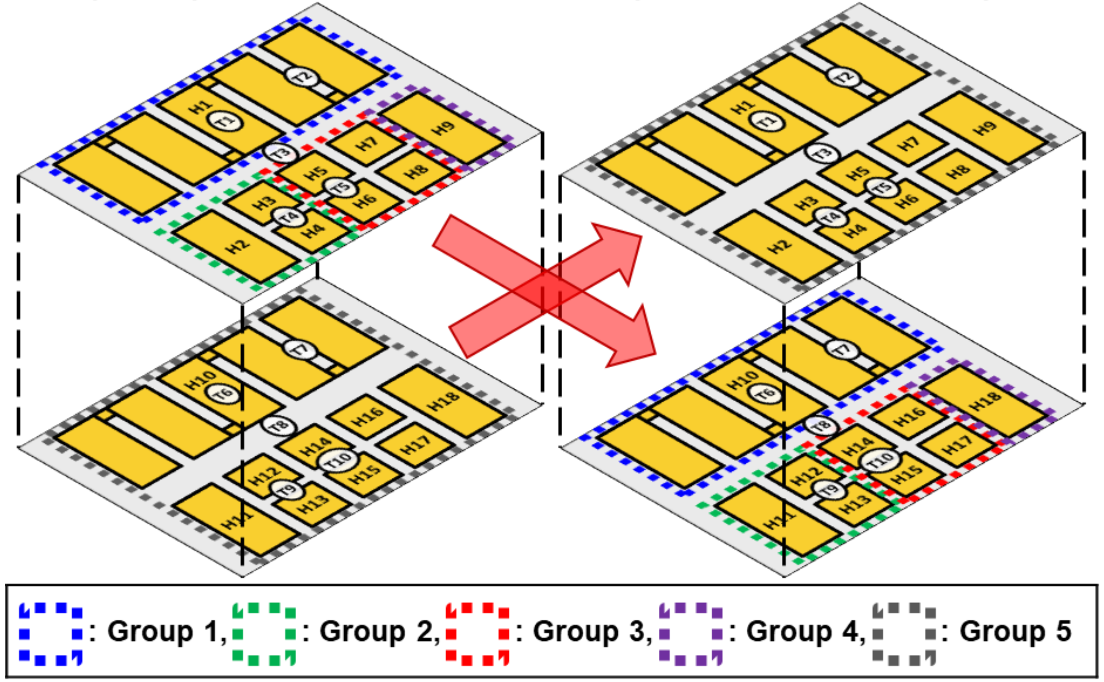
Ref2: 10.1109/ECTC51906.2022.00169

PKG-level Thermal Management Tests

PKG-level Test

Approach 1:
Top Floorplan, Bottom Uniform

Approach 2:
Top Uniform, Bottom Floorplan

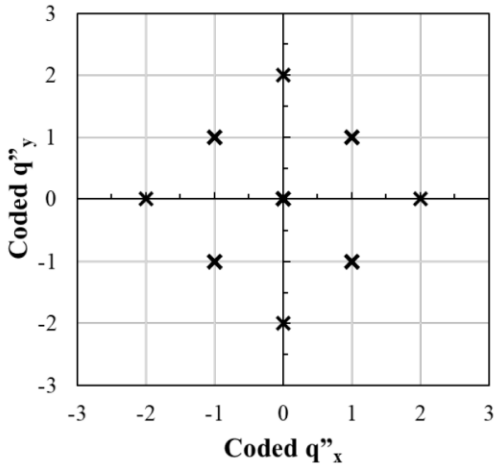


Each heater group is boxed by dashed-rectangles in different colors

Approach 1 & 2 : investigate the effect of joint gap between top/bottom dies on thermal behavior of the 3DIC TTV

Table 1. Coded values of the input parameters for the central composite design (CCD) (x ≠ y)

RSM design	Coded values				
Heat flux of j^{th} heater group	-2	-1	0	1	2
q''_1	0.1	0.2	0.3	0.4	0.5
q''_2	0.2	0.425	0.65	0.875	1.1
q''_3	0.2	0.425	0.65	0.875	1.1
q''_4	0.2	0.425	0.65	0.875	1.1
q''_5	0.1	0.2	0.3	0.4	0.5

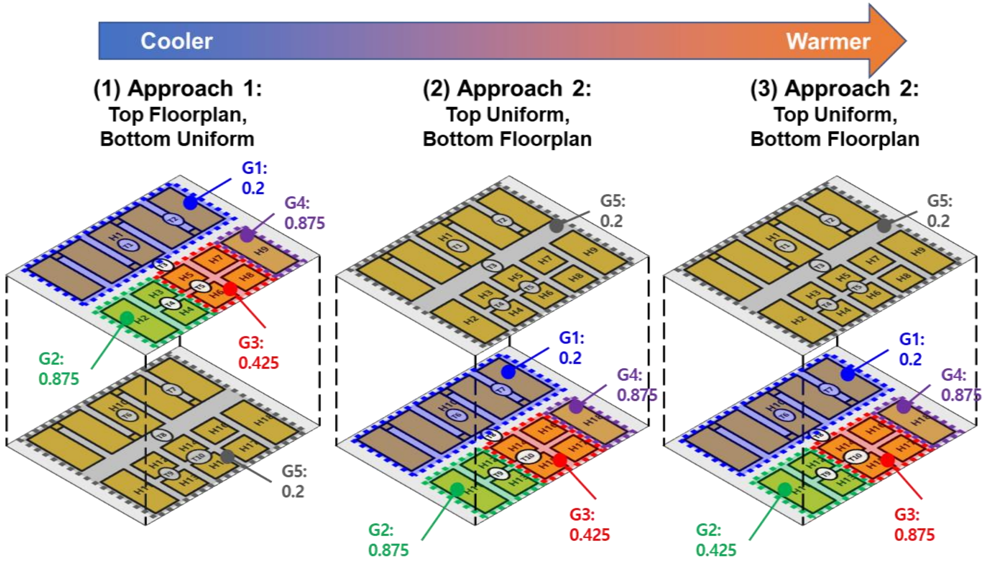


Coded values of each heater group's q" w.r.t. their actual values. A coded value, -2, corresponds to the minimum, and a coded value, +2, corresponds to the maximum of each heater group's heat flux.

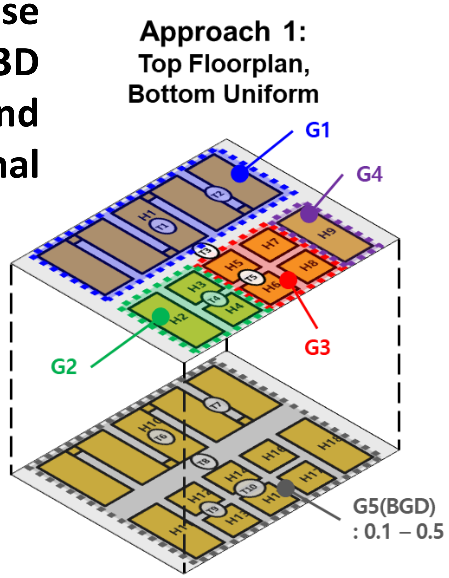
Ref2: 10.1109/ECTC51906.2022.00169

PKG-level Thermal Management Tests

PKG-level Test



Thermal response model of the 3D IC utilized to find thermally optimal floorplan



Step 1) Define input constraints:

Ex) $q''_{BGD} = 0.3W/mm^2$, $P_{total} = 45W$

Step 2) Explore possible power combinations in G1 through G4

i) Determine dynamic range of each heater group's power (or power density)

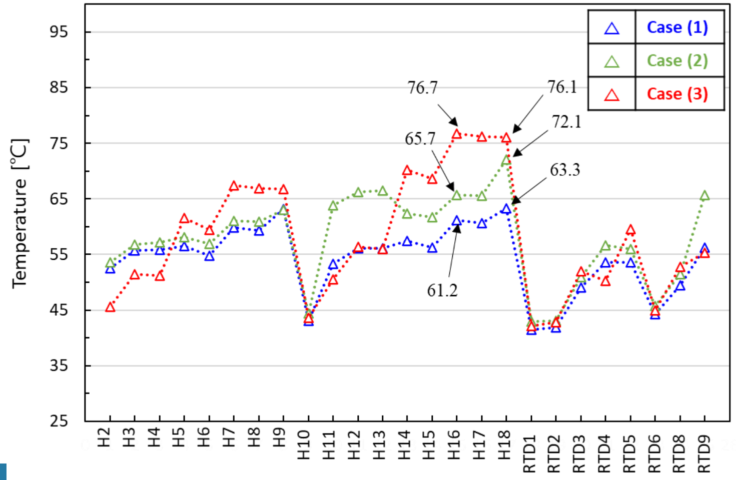
ii) Divide the dynamic range into multiple discrete power (or power density) steps

iii) Explore DOE of heater groups' power (or power density) and check whether the sum of each heater's power is equivalent to target P_{total}

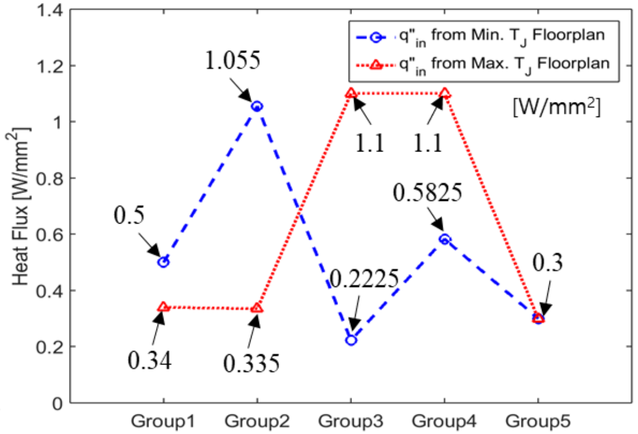
Step 3) Find a thermally optimized floorplan by checking $T_{junction}$

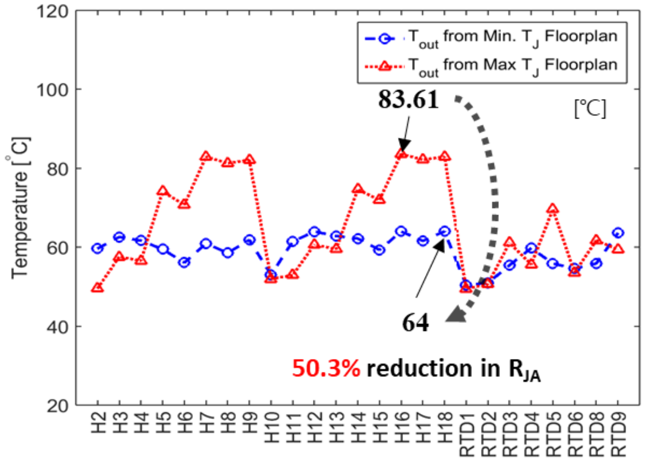
i) Store $T_{junction}$ from every possible floorplan from Step 2

ii) Find a floorplan among others to show the smallest $T_{junction}$, and this floorplan is the thermally optimized floorplan of interest



$T_{junction}$ getting higher as the joint-gap & floorplan effects are accumulated



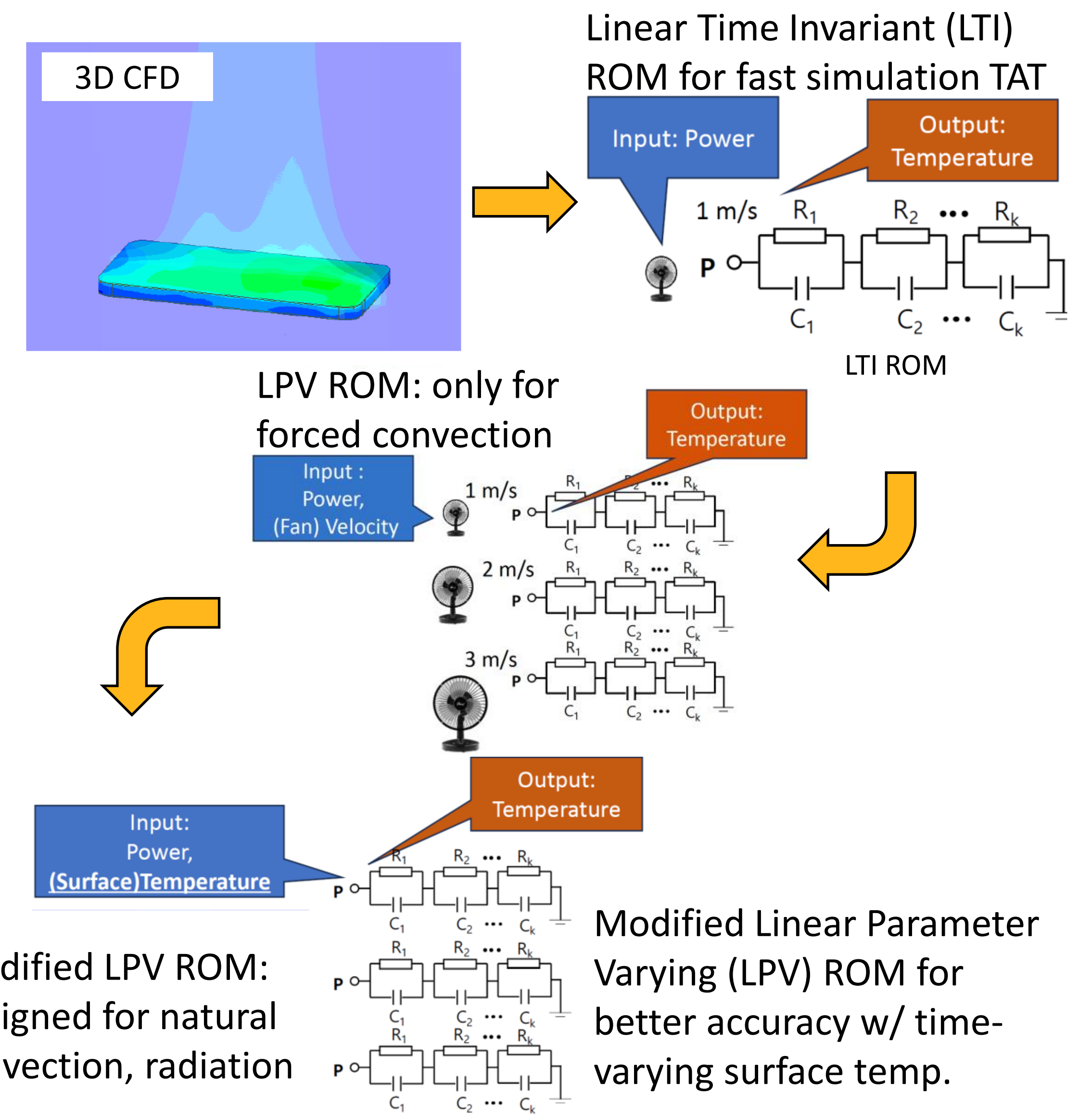


Ref2: 10.1109/ECTC51906.2022.00169

Set-level LPV ROM Validation Effort

Needs for “Fast & Accurate” Simulation

- Traditional 3D CFD is too slow to estimate benchmark performance → Need for “Fast” Sim.
- LTI ROM is not applicable for time varying boundary condition
- LPV ROM is can be used for forced convection, but not for natural convection and radiation
- Therefore, a Modified LPV ROM is suggested for natural convection & radiation conditions



Linear Time Invariant (LTI) ROM for fast simulation TAT

LPV ROM: only for forced convection

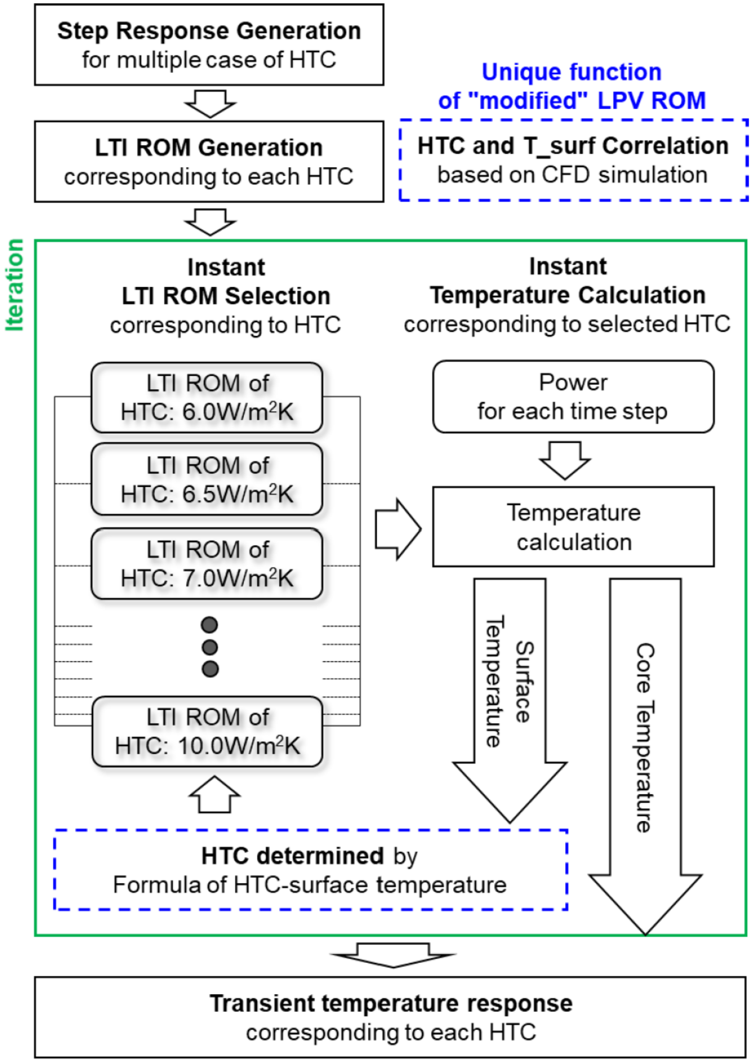
Modified LPV ROM: designed for natural convection, radiation

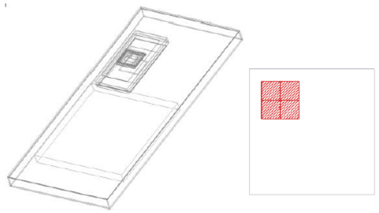
Modified Linear Parameter Varying (LPV) ROM for better accuracy w/ time-varying surface temp.

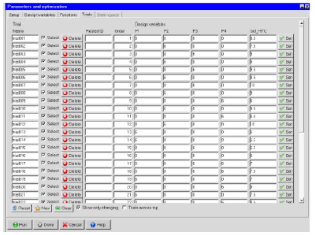
Ref3: 10.1109/ITherm55368.2023.10177511

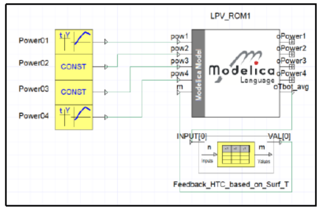
Set-level LPV ROM Validation Effort

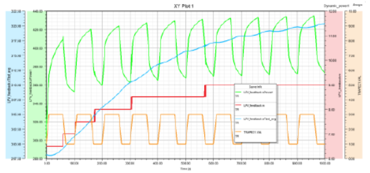
Ref3: 10.1109/ITherm55368.2023.10177511











[Preparation]

Icepak CFD Setup of Smartphone

- Model Setup
- Extract surface temperature dependent HTC of external surfaces of smartphone

[Preparation]

Icepak – Training Data for LPV ROM

- Transient Trials depending on various HTC

[Preparation/Evaluation]

Twin Builder – Use of LPV ROM

- LPV ROM Wizard for ROM generation
- LPV ROM evaluation

[Result]

Icepak – Validation Scenario(s)

- Comparison LPV ROM with ICEPAK CFD

Fast

Use instant LTI ROM during temp. calculation

Accurate

Update LTI ROM based on B.C. (HTC)

Surface Temp. (n) → HTC (n) → LTI ROM (n+1)

(n: nth time step)

1st correlation through CFD

Hottest surface temperature vs. Hottest surface HTC

2nd correlation through CFD

Hottest surface HTC vs. Other surface HTCs

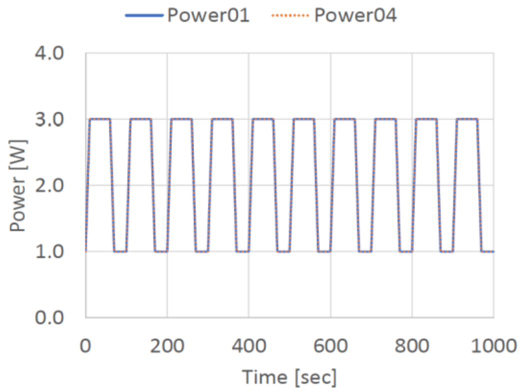
*LTI ROM: Linear Time-Invariant Reduced Order Model

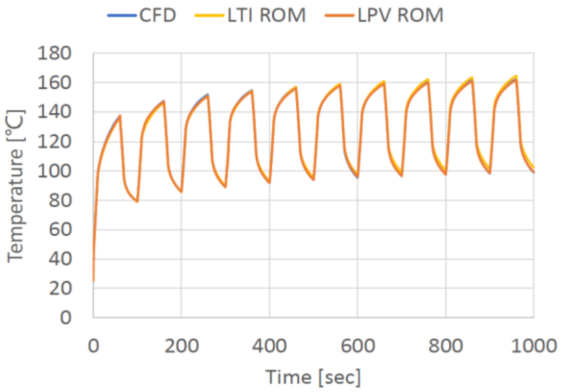
**LPV ROM: Linear Parameter-Varying Reduced Order Model

Set-level LPV ROM Validation Effort

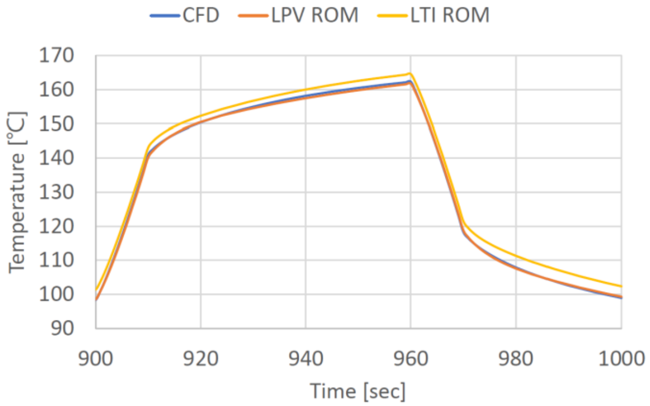
Set-level Validation

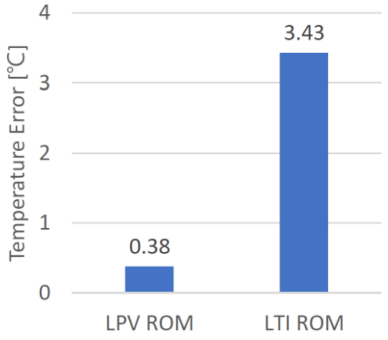
- Periodic Power Change Scenario for a Particular Core
  - 3W for 30 sec / 1W for 20 sec to core 1 and core 4 for 1000 seconds



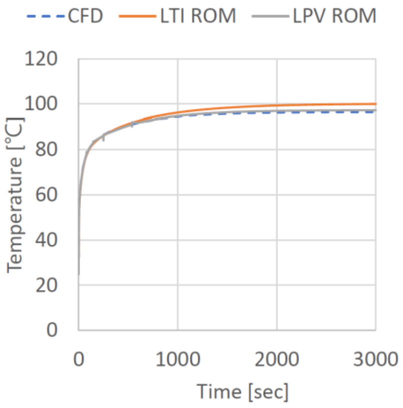


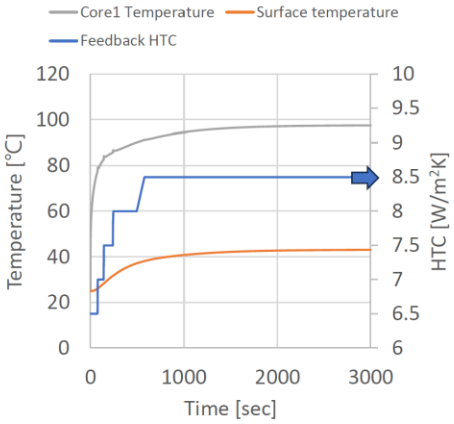
- Temperature Error : LPV ROM 0.4℃ vs. LTI ROM 3.4℃

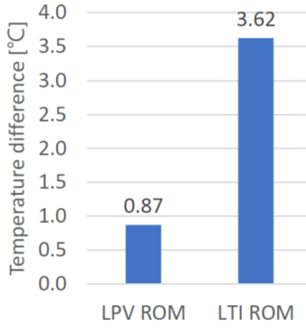




- Uniform Power Scenario
  - 3W for 3000 seconds
  - Temperature Error : LPV ROM 0.9℃ vs. LTI ROM 3.6℃







	LPV ROM	CFD
Training cases	36 cases	-
Preparation (ROM build-up)	43 hr 11 min	-
Iteration (Solving)	5.8 s	13 hr 36 min
Total elapsed time		
1x	43.2 hr	13.6 hr
10x	43.2 hr	136 hr
100x	**43.3 hr**	**1360 hr**

	Workstation specification
CPU processor	Intel(R) Xeon(R) Gold 6230R CPU @ 2.10GHz 2.10 GHz (2 processors)
RAM	512GB
Used core in parallel	40ea

Ref3: 10.1109/ITherm55368.2023.10177511

References

[1] K. W. Jung, E. Hwang, J. Seomun and S. Kim, "A Time and Cost-Efficient Design Methodology to Estimate Effective Thermal Conductivities in System-on-Chips with Composite Materials," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 192-199, doi: 10.1109/ECTC51909.2023.00041.

[2] K. W. Jung, E. Cho, S. Jo, S. Ryu, J. Kim and D. K. S. Oh, "Assessment of Thermal-aware Floorplans in a 3D IC for Server Applications," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 1036-1047, doi: 10.1109/ECTC51906.2022.00169.

[3] Y. Im, G. Jung, M. Lee, A. Gangrade and S. Kim, "Thermal Modeling and Optimization of Mobile Device using modified LPV ROM," 2023 22nd IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), Orlando, FL, USA, 2023, pp. 1-8, doi: 10.1109/ITherm55368.2023.10177511.

Efficient and Innovative Thermal Management for Power Hungry AI/ ML Applications: Challenges and Opportunities

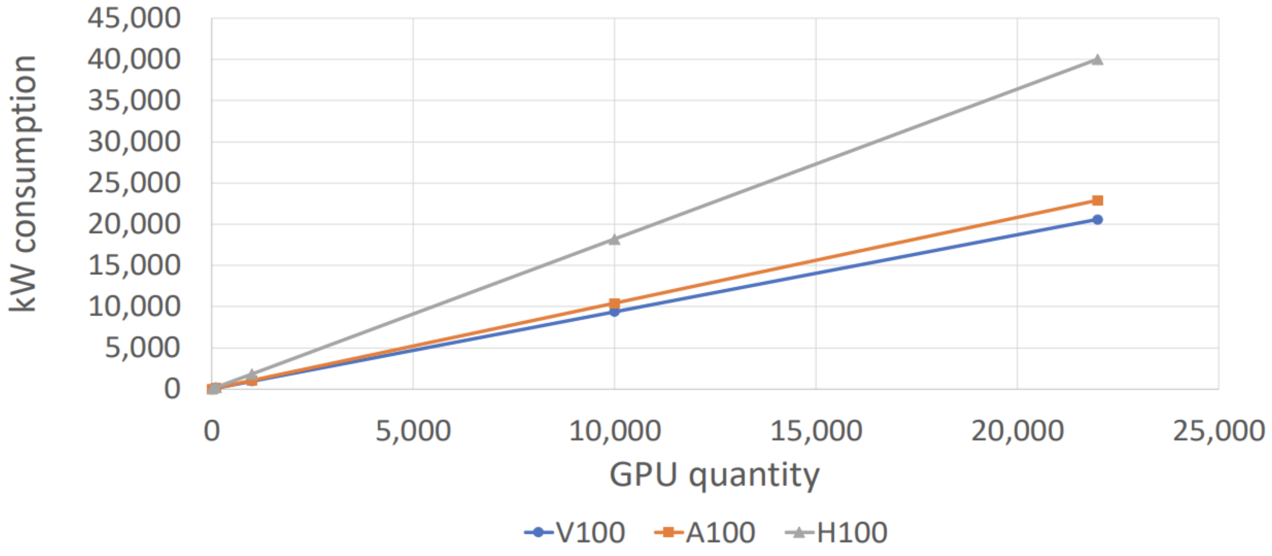
Mudasir Ahmad

Disclaimer:
The information outlined in these slides are not official Google Communication or Position

Contents

AI/ML Power Consumption Trajectory

Schneider Electric estimate	2023	2028
Total data center power consumption	57 GW	93 GW
AI power consumption	4.5 GW	14.0-18.7 GW
AI power consumption (% of total)	8%	15-20%
AI workload (Training vs Inference)	20% Training, 80% Inference	15% Training, 85% Inference
AI workload (Central vs Edge)	95% Central, 5% Edge	50% Central, 50% Edge

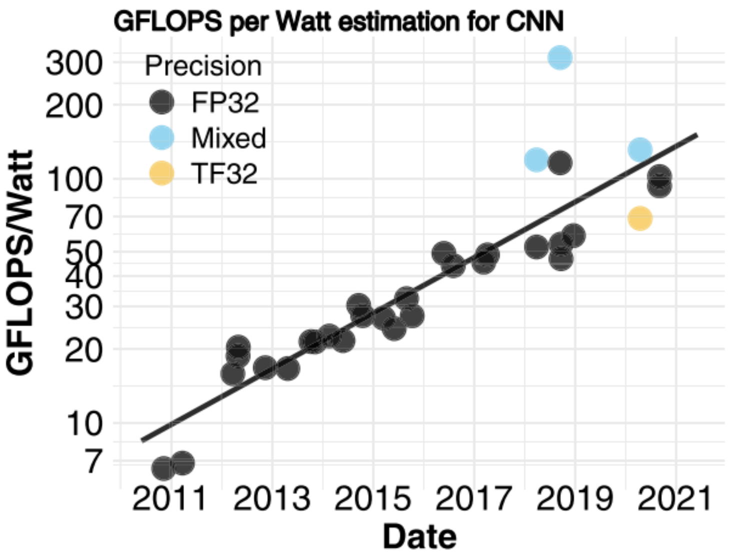


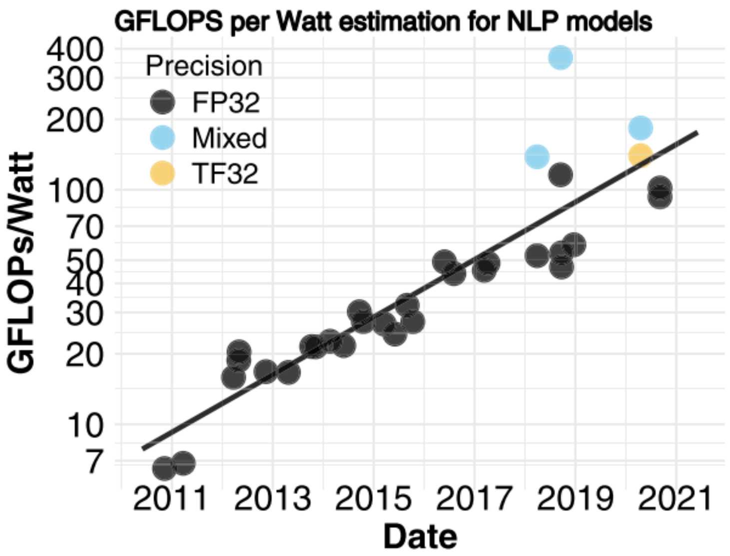
GPU	TDP (W)[11]	TFLOPS[12] (Training)	Performance over V100	TOPS[13] (Inference)	Performance over V100
V100 SXM2 32GB	300	15.7	1X	62	1X
A100 SXM 80GB	400	156	9.9X	624	10.1X
H100 SXM 80GB	700	500	31.8X	2,000	32.3X

Next Gen Nvidia Systems will be liquid cooled

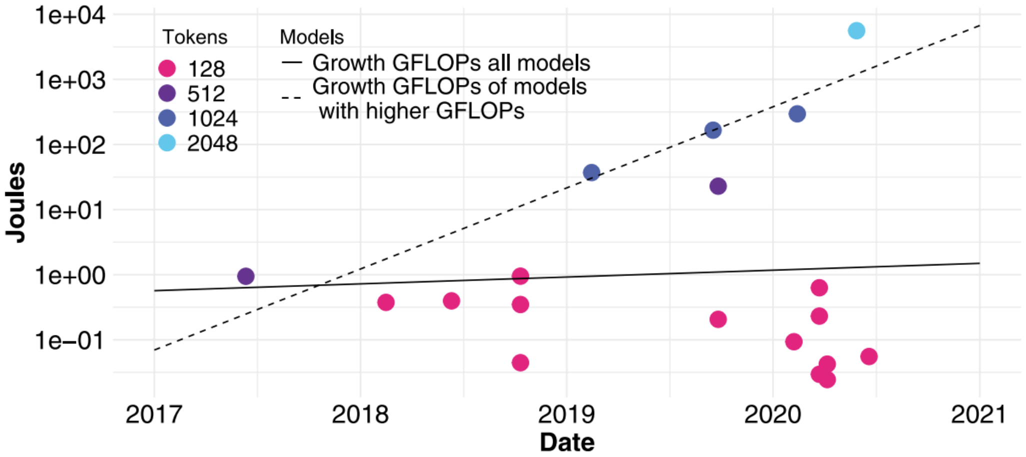
Reference: Schneider Electric

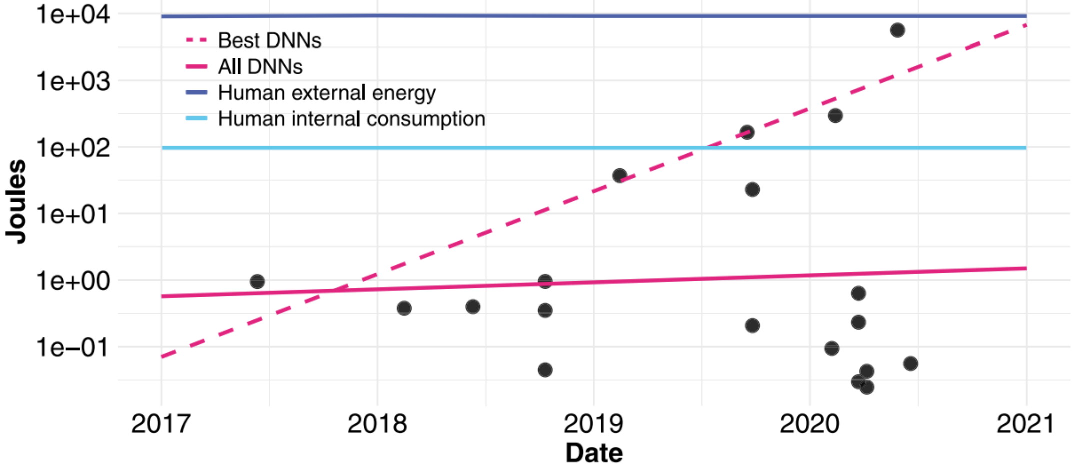
AI/ML Power Consumption Trajectory


GFLOPS per Watt estimation for CNN


GFLOPS per Watt estimation for NLP models

- •Hardware efficiency is improving significantly
- •However, power consumption is still increasing overall
- •Even with hardware improvements, systems are still very power hungry



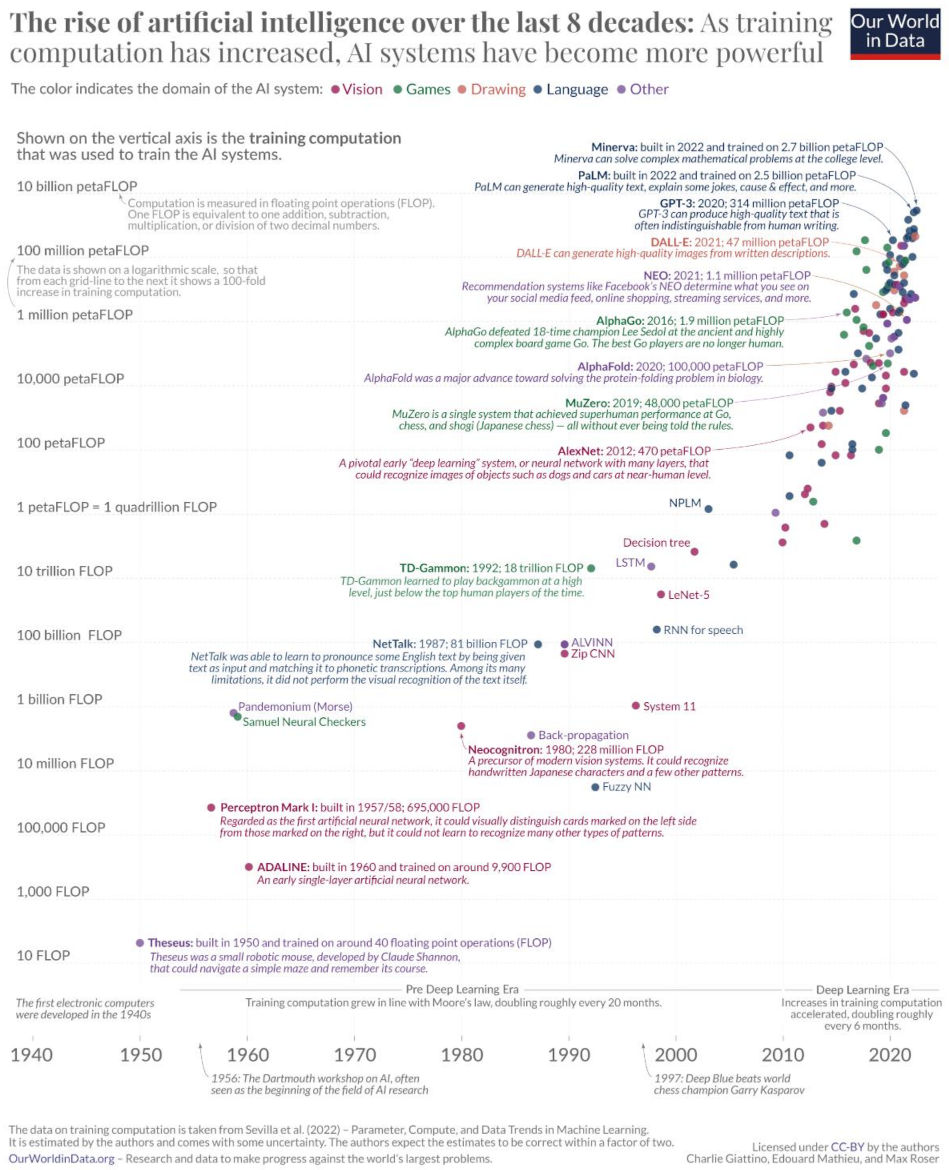


R. Desislavov, “Trends in AI inference energy consumption: Beyond the performance-vs-parameter laws of deep learning”, Sustainable Computing: Informatics and Systems, 2023

AI/ML Software Trajectory

- From 2010 - 2020, AI/ML algorithms have grown exponentially
- Algorithms could rapidly evolve from one approach to another
- Different categories evolving rapidly for different applications
- Faster evolution than Hardware Development timescales
- AI/ML software evolving every 8 months*

*Ho, A; Besiroglu, T; "ALGORITHMIC PROGRESS IN LANGUAGE MODELS" 2024



The rise of artificial intelligence over the last 8 decades: As training computation has increased, AI systems have become more powerful

The data on training computation is taken from Sevilla et al. (2022) – Parameter, Compute, and Data Trends in Machine Learning. It is estimated by the authors and comes with some uncertainty. The authors expect the estimates to be correct within a factor of two.
OurWorldinData.org – Research and data to make progress against the world's largest problems.

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AI/ML Thermal Challenges

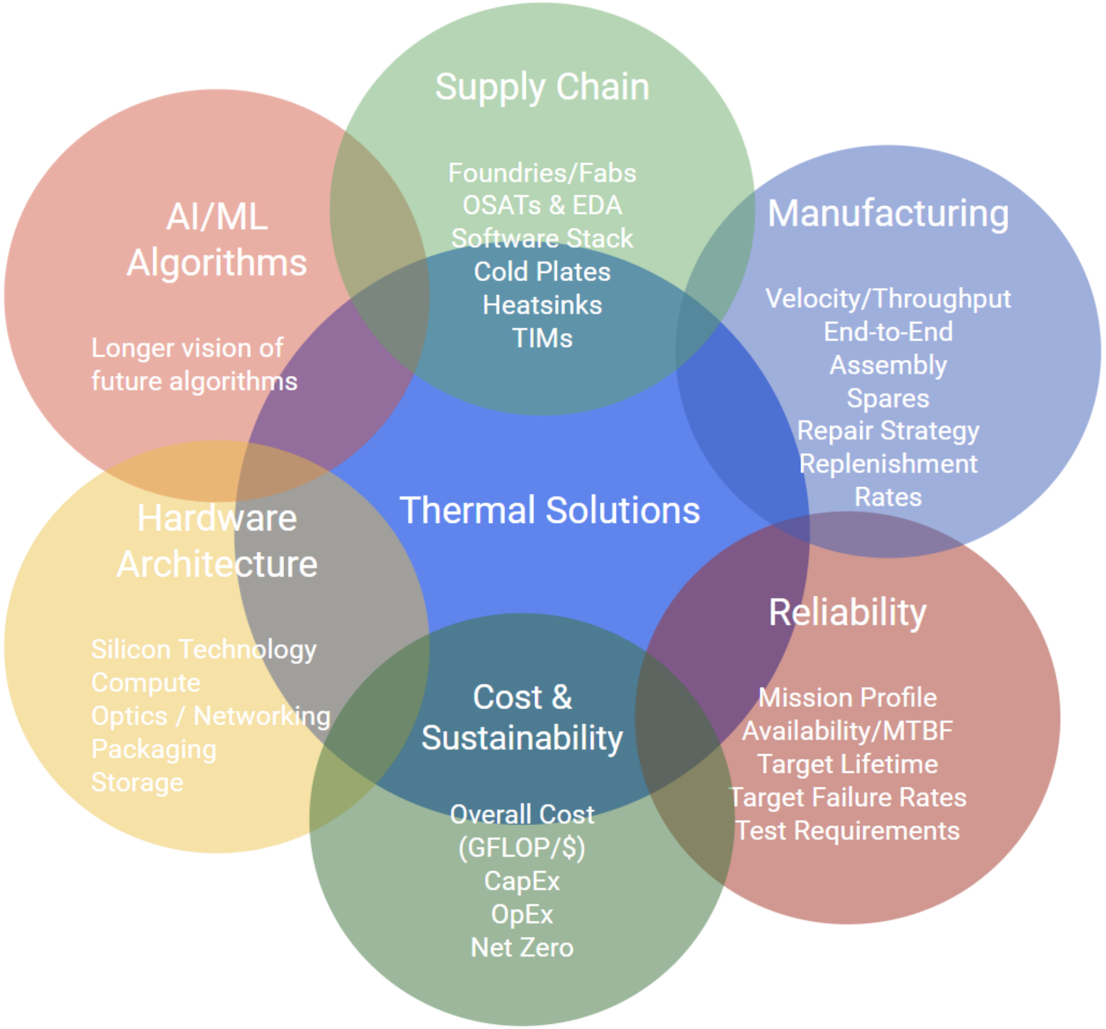
AI/ML hardware is an entire *system* - not just a chip

A specific thermal solution may be great

But…is it:

- Reliable?
- Manufacturable?
- Compatible with existing technologies?
- Cost Effective?
- Aligned with future hardware roadmap?
- Etc.

Thermal solutions need to be optimized for scale across multiple dimensions



Supply Chain
Foundries/Fabs
OSATs & EDA
Software Stack
Cold Plates
Heatsinks
TIMs

AI/ML Algorithms
Longer vision of future algorithms

Manufacturing
Velocity/Throughput
End-to-End
Assembly
Spares
Repair Strategy
Replenishment Rates

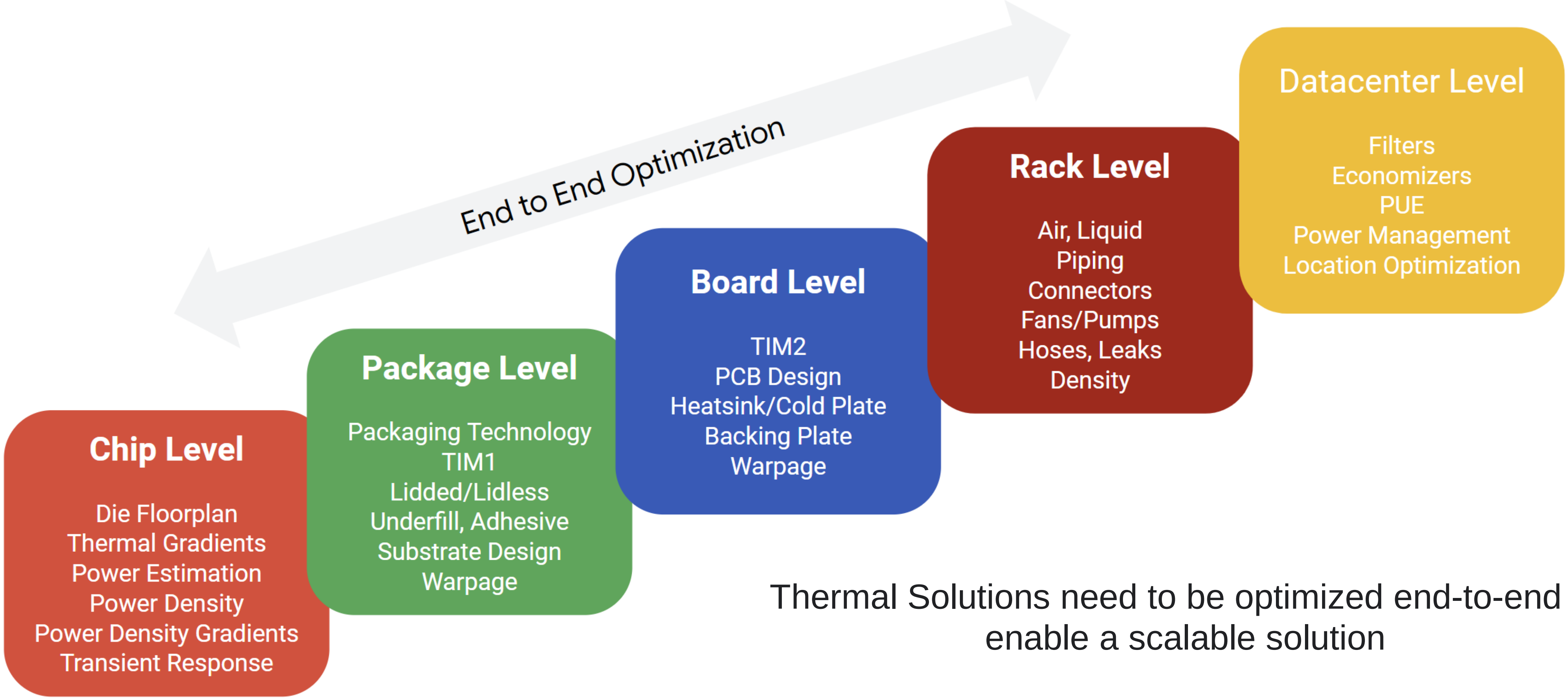
Thermal Solutions

Hardware Architecture
Silicon Technology
Compute
Optics / Networking
Packaging
Storage

Reliability
Mission Profile
Availability/MTBF
Target Lifetime
Target Failure Rates
Test Requirements

Cost & Sustainability
Overall Cost (GFLOP/$)
CapEx
OpEx
Net Zero

Thermal Design Parameters



End to End Optimization

Chip Level

Die Floorplan
Thermal Gradients
Power Estimation
Power Density
Power Density Gradients
Transient Response

Package Level

Packaging Technology
TIM1
Lidded/Lidless
Underfill, Adhesive
Substrate Design
Warpage

Board Level

TIM2
PCB Design
Heatsink/Cold Plate
Backing Plate
Warpage

Rack Level

Air, Liquid
Piping
Connectors
Fans/Pumps
Hoses, Leaks
Density

Datacenter Level

Filters
Economizers
PUE
Power Management
Location Optimization

Thermal Solutions need to be optimized end-to-end to enable a scalable solution

This means EACH design is unique and needs to be optimized independently

Thermal Solution Decision Making Framework - SPARCS

(S)chedule	Can this solution be implemented at scale for the current planned deployment schedule?
(P)rocess	Does a manufacturing process/workflow exist for it to the deployed at scale?
(A)lternatives	Do viable, scalable alternatives exist if this does not work? Are they production ready?
(R)eliability	What is the reliability of the solution relative to others? Does it meet or exceed the reliability Requirements?
(C)ost	Is the solution end-to-end cost effective?
(S)ustainability	Is the solution sustainable from a net zero perspective?

Standardization Opportunities

- Where possible, standardization speeds up product development, reduces cost and enables rapid scaling

- Potential Opportunity Examples:
  - Reliability Testing of Thermal Interface Materials
  - Quick connect/disconnect interface specifications and reliability testing
  - Pump specifications and reliability testing
  - Coolant specifications and reliability testing
  - Cold Plate specifications and reliability testing
  - Common testing software specifications

OCP Cooling Environments Project is an example of such an effort

Opportunities for Advanced Packaging

- Several opportunities for holistic thermal performance enhancement of advanced packaging

Algorithms

Experimentally validated die thermal hotspot prediction - 1D, 2.5D, 3D Packaging
More accurate TDP prediction
Die thermal hotspot optimization - including die warpage post PCBA SMT
TIM1/1.5/2 reliability prediction - pumpout, dryout, voiding etc.
Die backside warpage prediction - post SMT
TIM BLT prediction - post PCBA SMT
Heatsink/Cold Plate attachment pressure prediction

Thermal

Innovative package level thermal solutions for high wattage and high thermal gradient applications - 1D, 2.5D, 3D Packaging
Higher thermal conductivity thermal interface materials
Thermal interface materials with reduced contact thermal resistance
Thermal solutions resistant to tolerance variations in high volume manufacturing

Reliability

CPI: Impact of TIM stiffness on package reliability
CPI: Impact of die layout on TIM reliability
CPI: Impact of heatsink/cold plate attachment on package and TIM reliability
Acceleration factors for TIM reliability, pre and post PCBA SMT
Impact of die level transient temperature changes on package and TIM reliability
Test methods for TIM1/1.5/2 reliability in field operating conditions
Impact of Liquid/Immersion Cooling on packaging reliability

Future is exciting…and uncertain

Algorithms	Could there be novel algorithms developed, that do not require such large power and chips to run?
Architecture	Could there be radical changes in architecture, resulting in a step function drop in power requirements?
Thermal Solutions	Could there be novel thermal solutions that simultaneously address large thermal gradients, high power density and fluctuations in a scalable way?

Significant cross-collaboration, research and development is needed
(and underway) in all these areas

Efficient and Innovative Thermal Management for Advanced Semiconductor Packaging

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Purdue University
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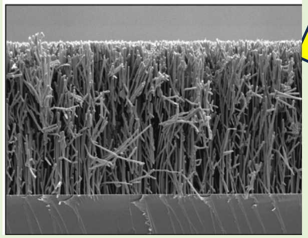
Semiconductor Packaging Laboratory

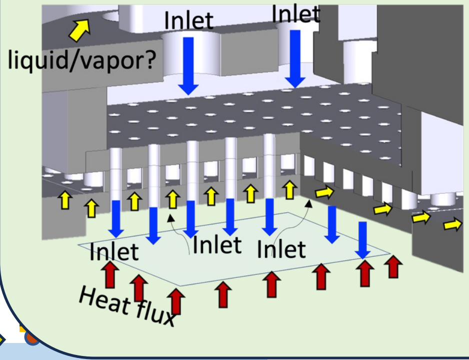
(All-in-one for Semiconductor Packaging, Heat transfer, and Assembly Lab)

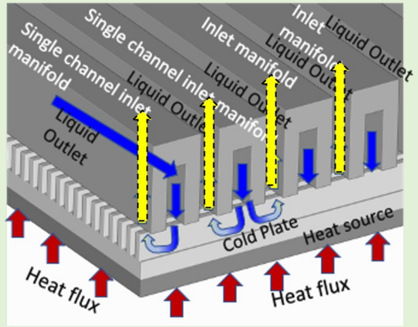
Thermal solutions for Heterogeneous 3D integration

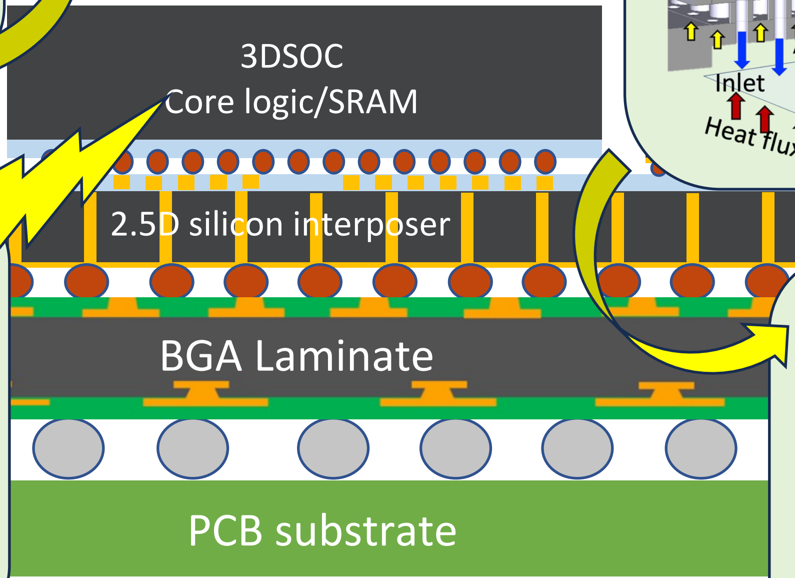
Interfaces: Diamond heat spreading material, CuNWs/PDMS based Thermal Interface Materials (TIMs)



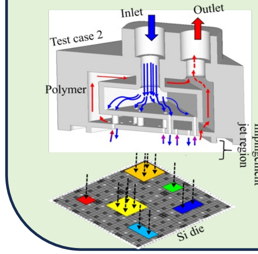
High heat fluxes: Direct-on-chip impingement jet cooling, embedded microchannel cooling, Inter-die microchannel cooling

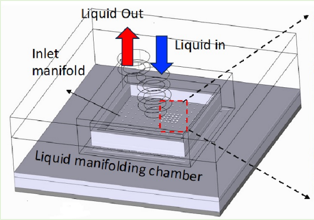


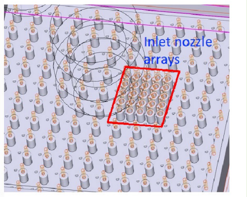




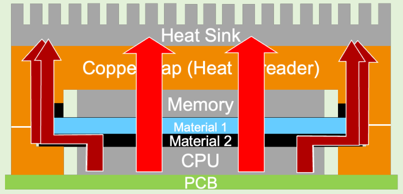
Hotspots: Hotspots targeted cooling approach, diamond heat spreading with local hotspots

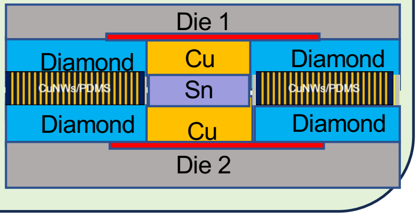




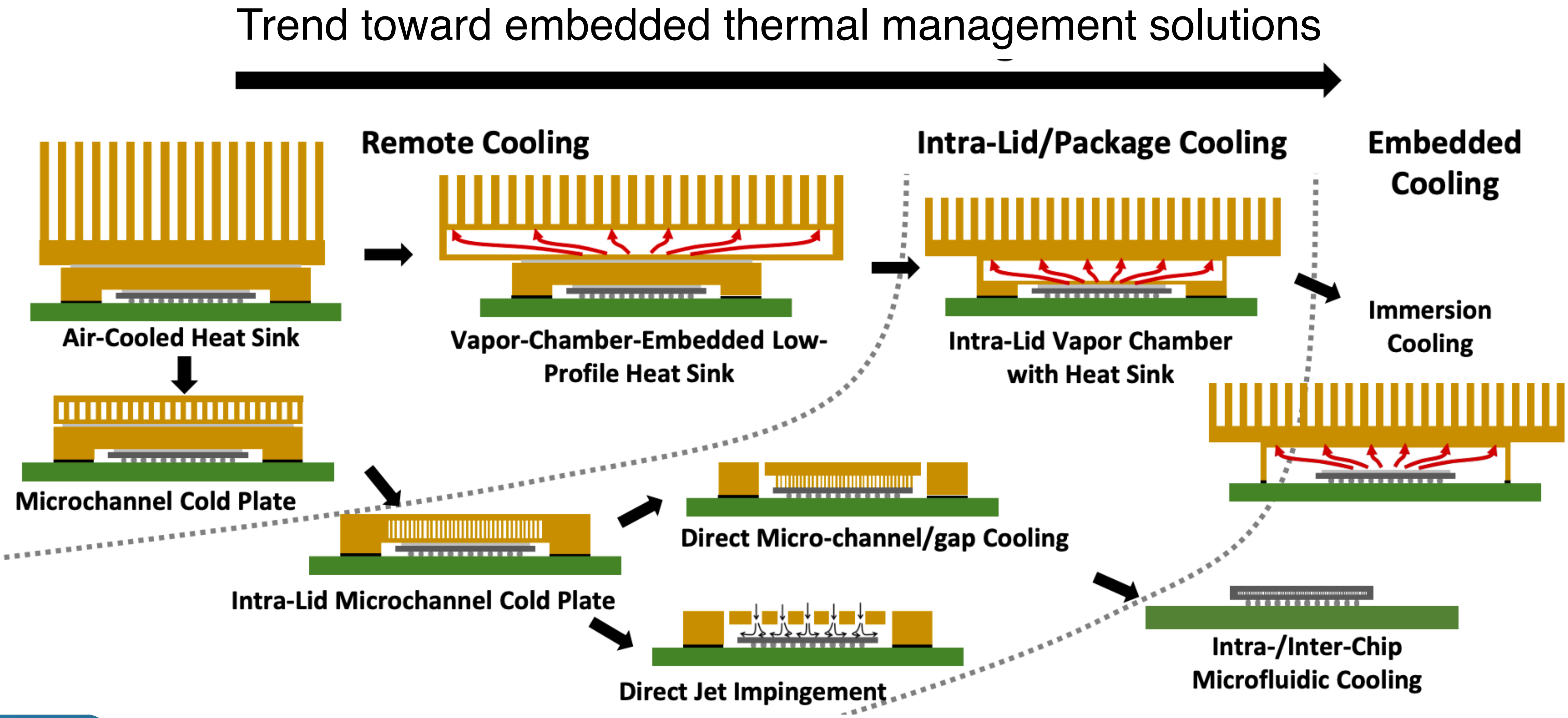


Thermal crosstalk: Thermal insulation materials, thermal heat spreading materials.





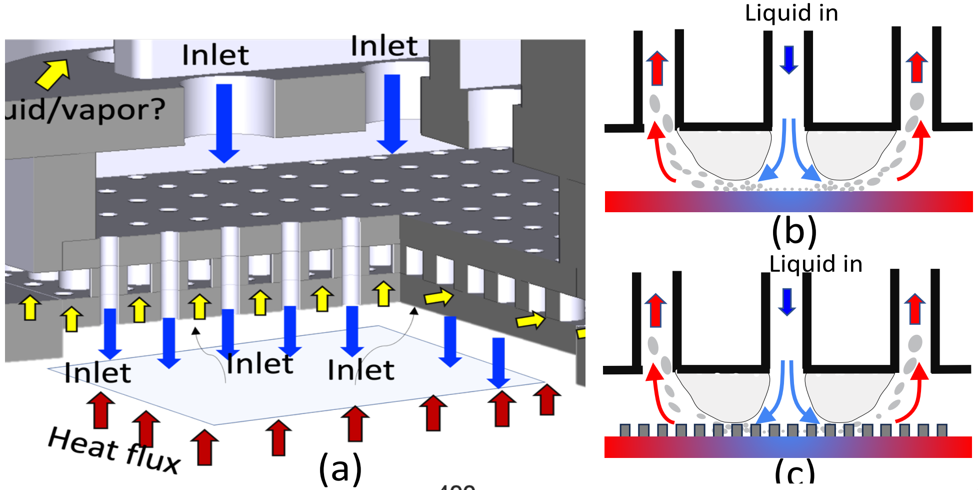
Integration of Advanced Thermal Solutions into the Heterogeneous Package

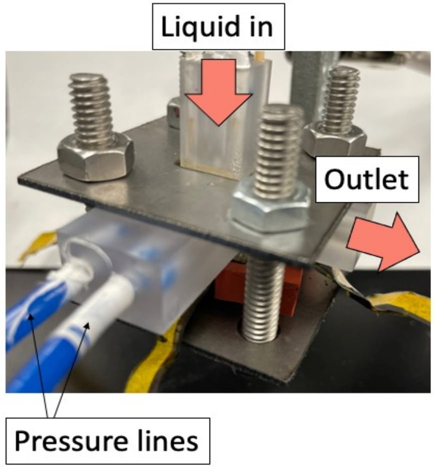


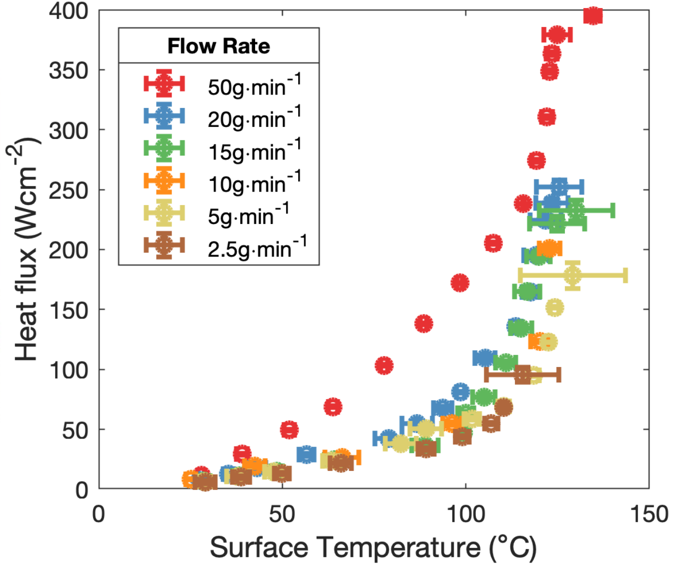
Courtesy to CTRC and Prof. Justin Weibel (Purude University)

Chip/Package Level Jet Impingement Cooling

Two-phase Jet Impingement Cooling on Micro-pin fins

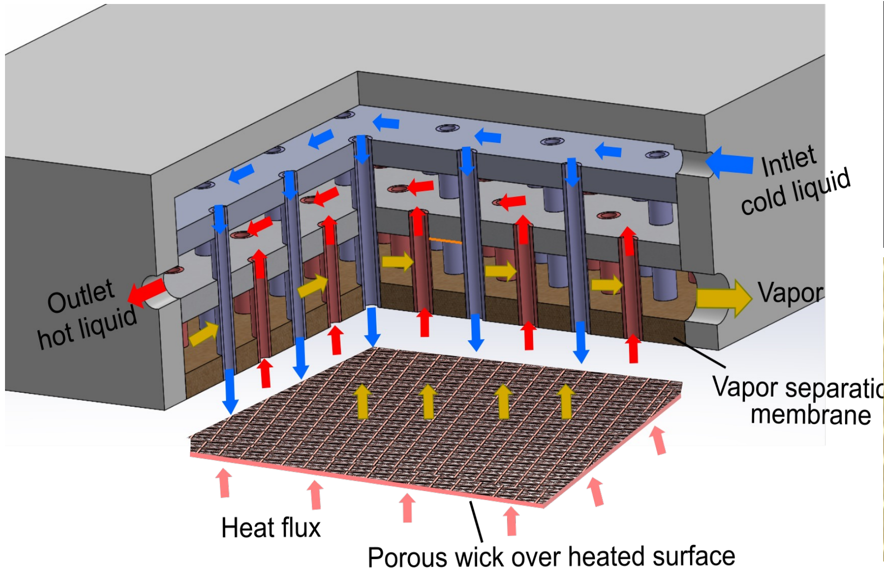


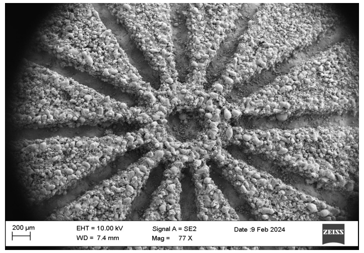




InterPACK 2023-Zheng, Wei.

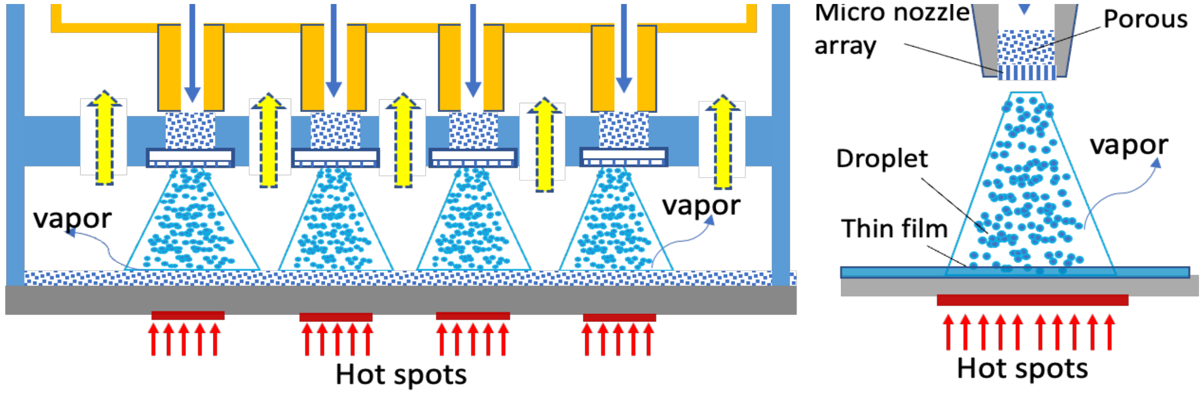
Two-phase Impingement Jet Cooling with Porous Wick





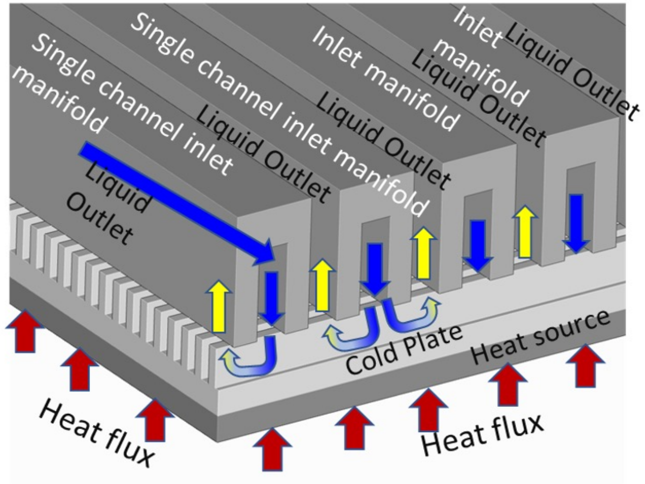
Credit to Prof. Scott from Binghamton University

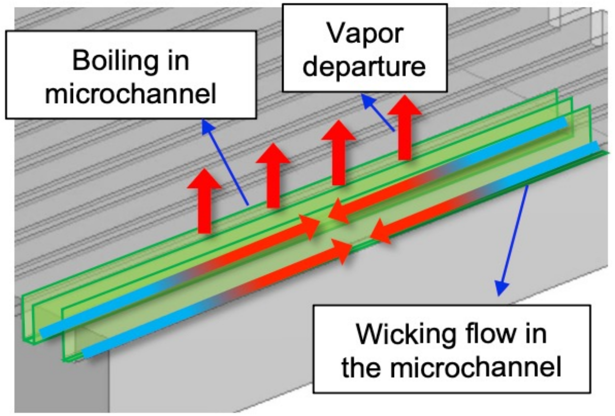
Low-Pressure Water Spray Impingement Cooling

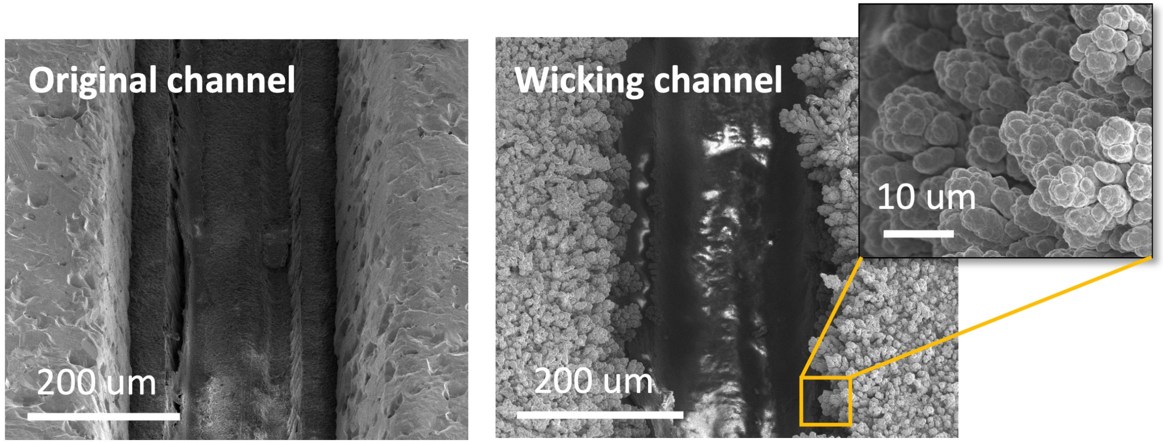


Chip/Package Level Microchannel Cooling

Capillary-driven Two-phase Embedded Microchannel

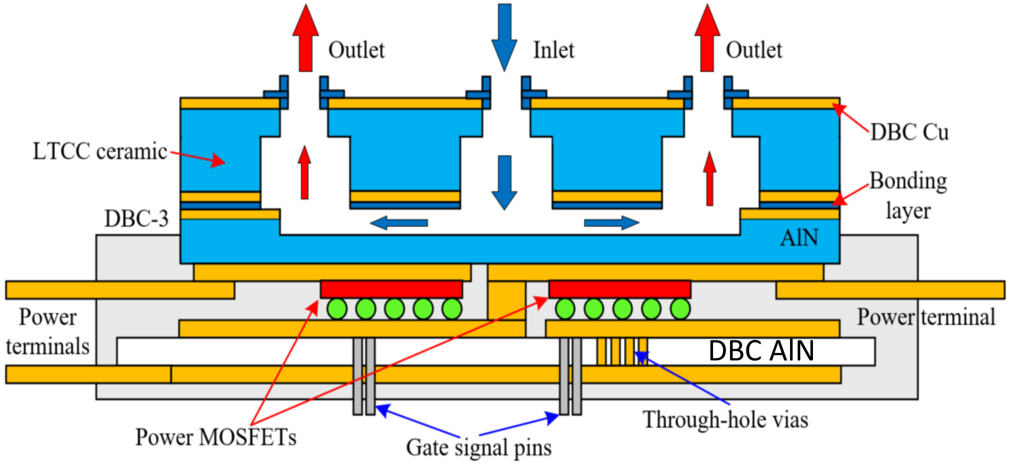


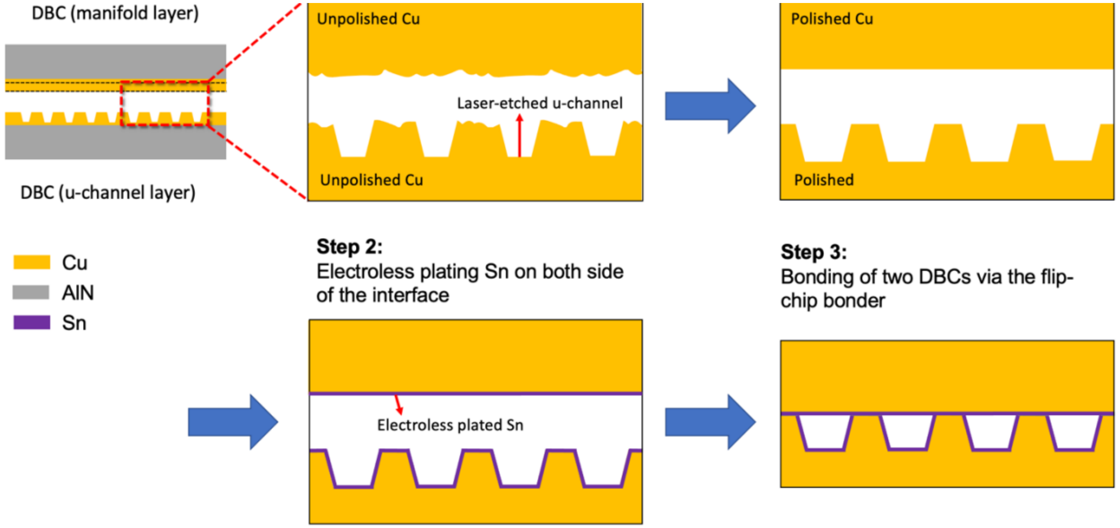




Lin, Wei, et al., APS 2023

AlN-bonded Embedded Microchannel Cooling

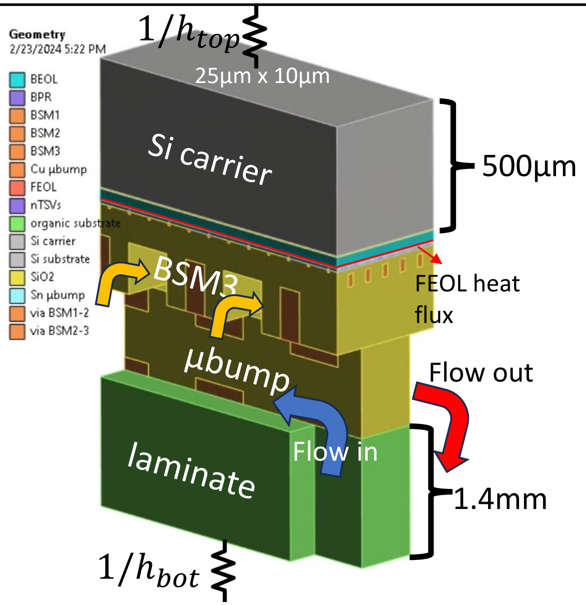




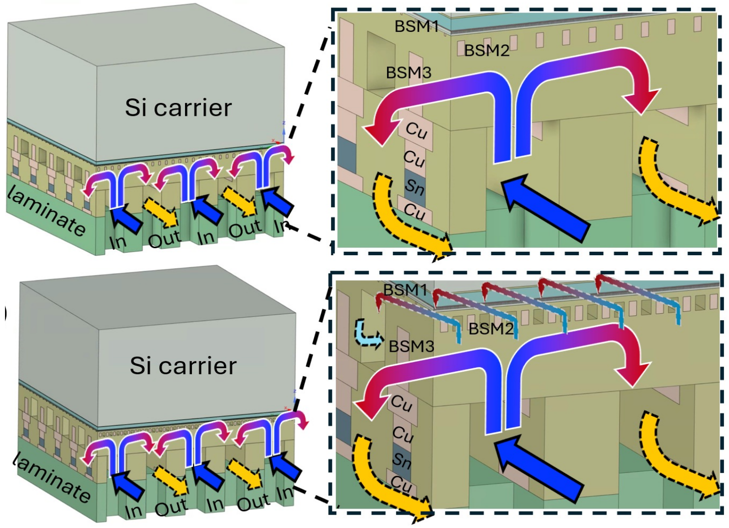
Lin, Wei, et al., JEP 2024

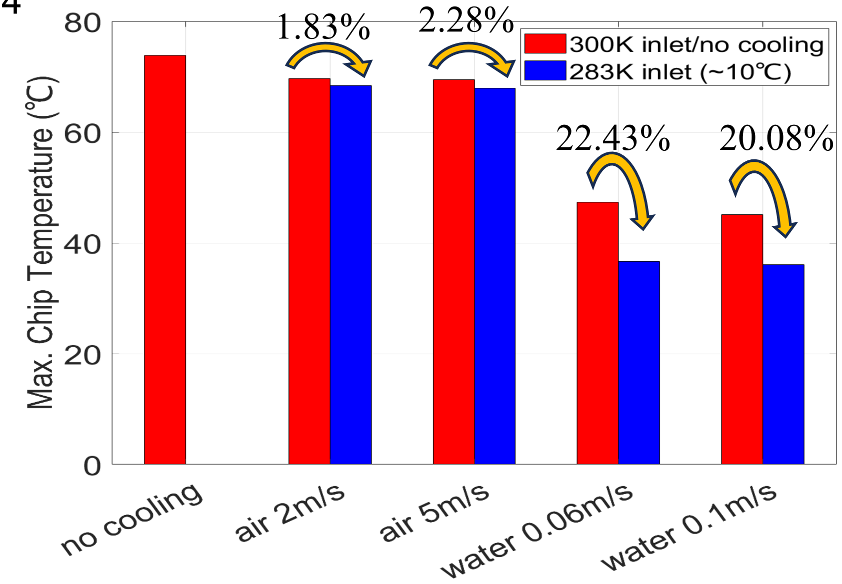
Intra-/Inter-Chip Microchannel Cooling

BEOL-based Embedded Microchannel cooling

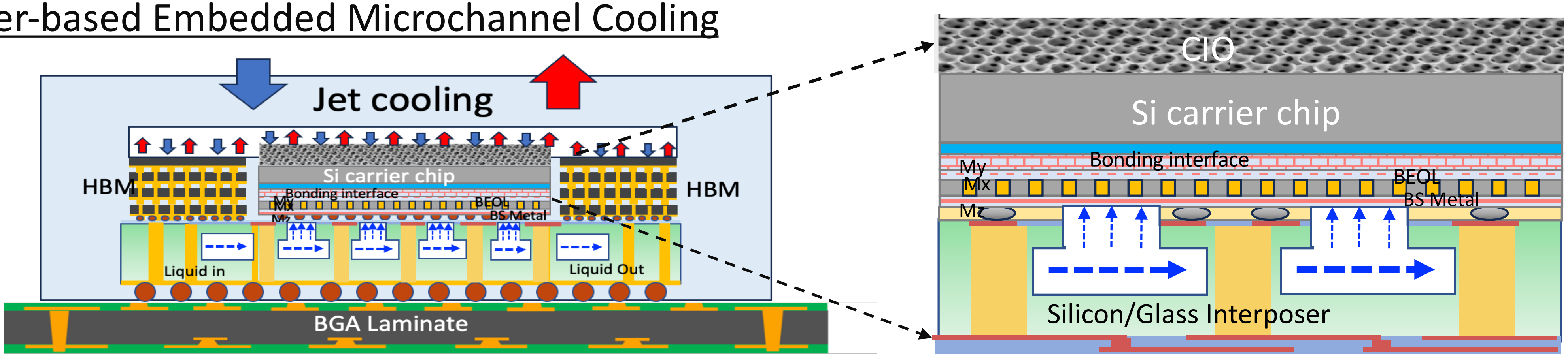


Xie, Wei, et al., ECTC 2024





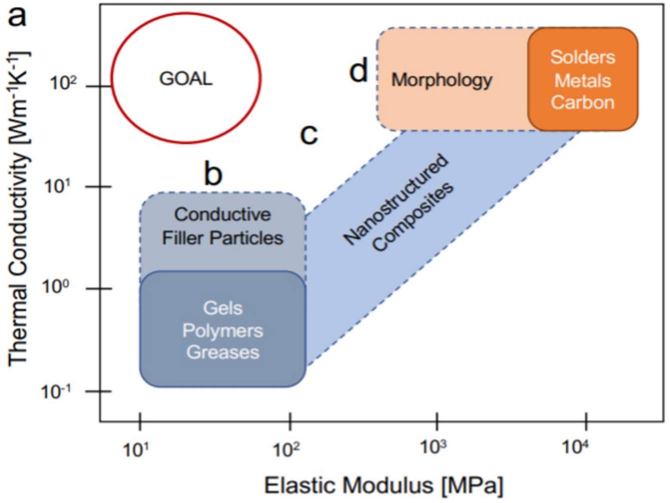
2.5D Interposer-based Embedded Microchannel Cooling

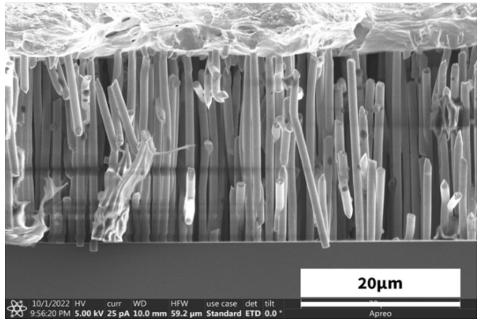


Xie, Wei, et al., ITherm 2024

Material Development for Thermal Management

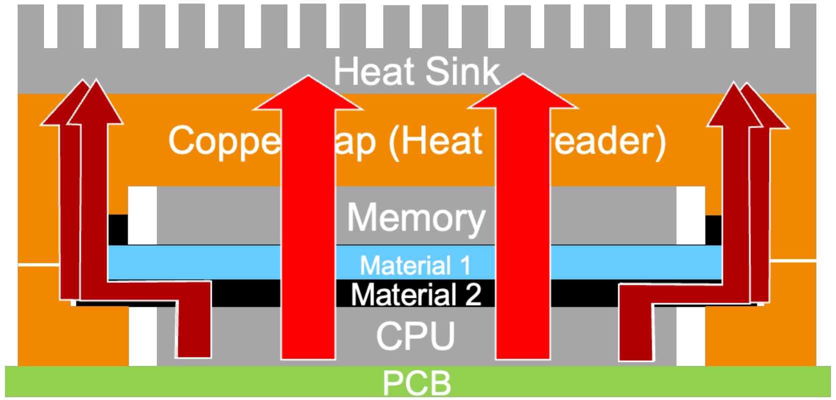
CuNWs/PDMS based Thermal Interface Materials (TIMs)



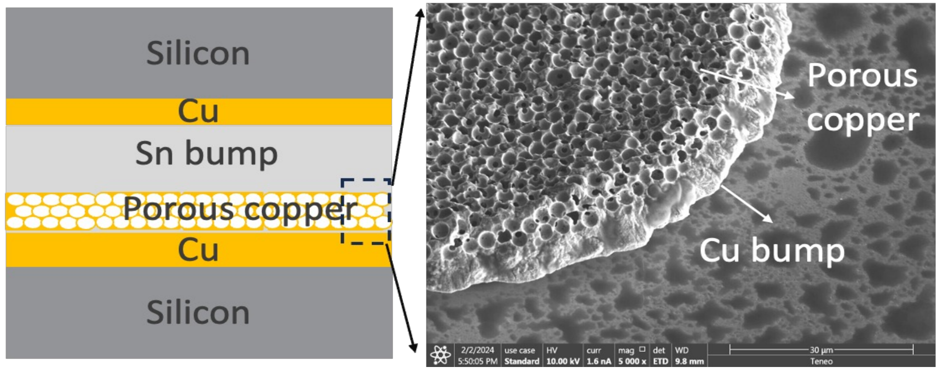


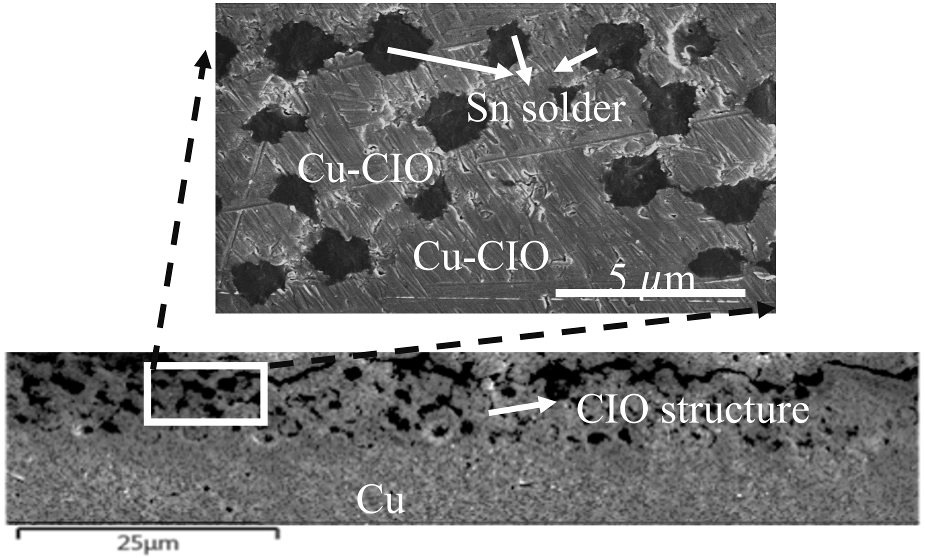
Qiao, Wei, et al., InterPACK 2023

Bi-layer materials with Heat Spreading and Thermal Insulation



Thermally-enhanced Micro-bump with Embedded Metal Structure





Wang, Wei, et al., ECTC 2024

Acknowledgement to collaborators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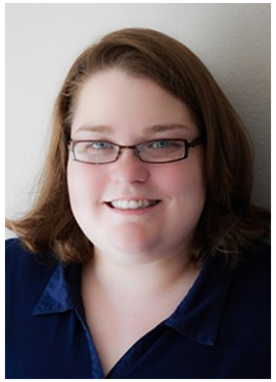
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Semiconductor Research Corporation

arpa·e

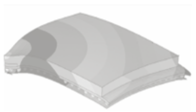
U.S. DEPARTMENT OF ENERGY

DARPA

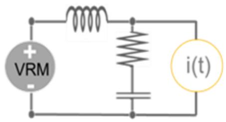
Thermal Simulation for 3DHI

Chris Ortiz, Ph. D.
Ansys

3DHI and Multi-Scale/Stage/Physics



Structural Integrity

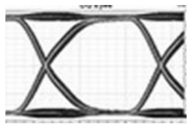


Power Integrity

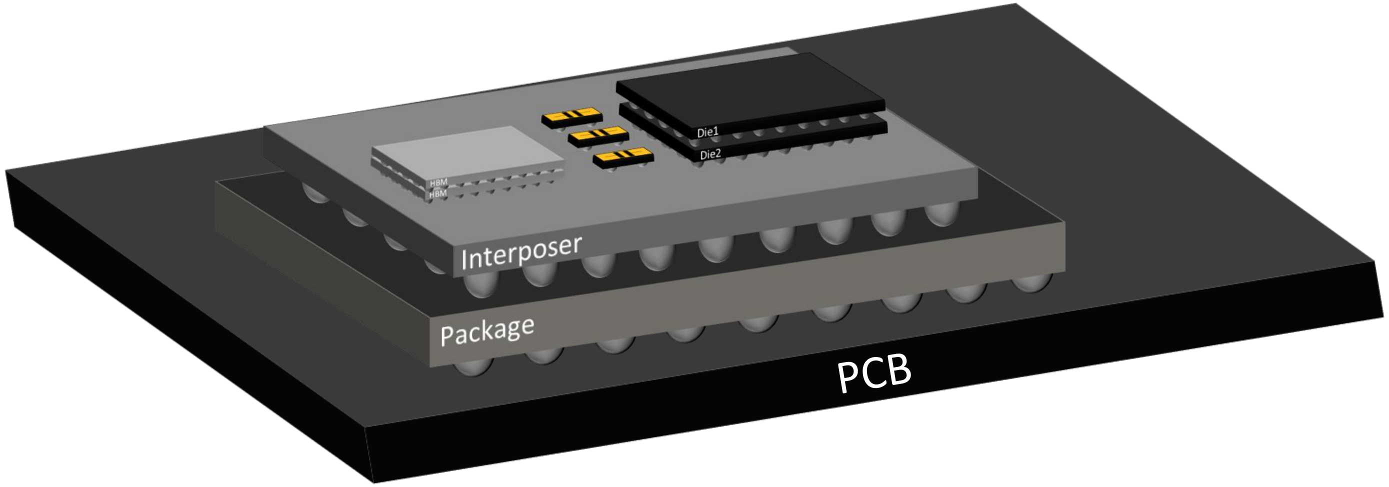
Physics
Interactions

Multiphysics

Thermal Integrity



Signal Integrity



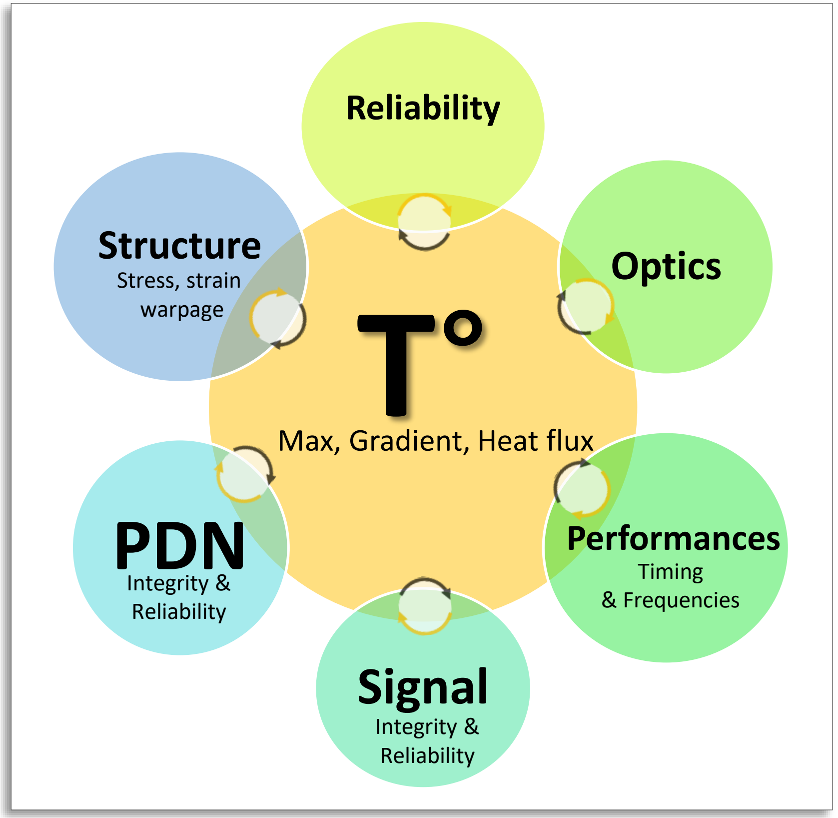
High capacity handling
Heterogeneous technologies
Complex Die stacking (billions of connections)

Feasibility the 3D-IC architecture

Increasing need for
Simulations
Multi-Physics
Multi-Stages
Multi-Layouts

SignOff the 3D-IC Implementation

Coupling of Physical Effects



Multiple Physics & Coupling

"New" topics for Semiconductors:

Thermal Integrity of Chiplet: T° and <u>many possible impacts</u>

Temperature vs. Timing…

Structural Integrity of Chiplet (Thermal stress)

Stress on device performance, reliability

Coupling of physics

Temperature is corner stone of coupling

Power and thermal runaway

Resistance and electromigration

Stress and coefficients of thermal expansion

Reliability

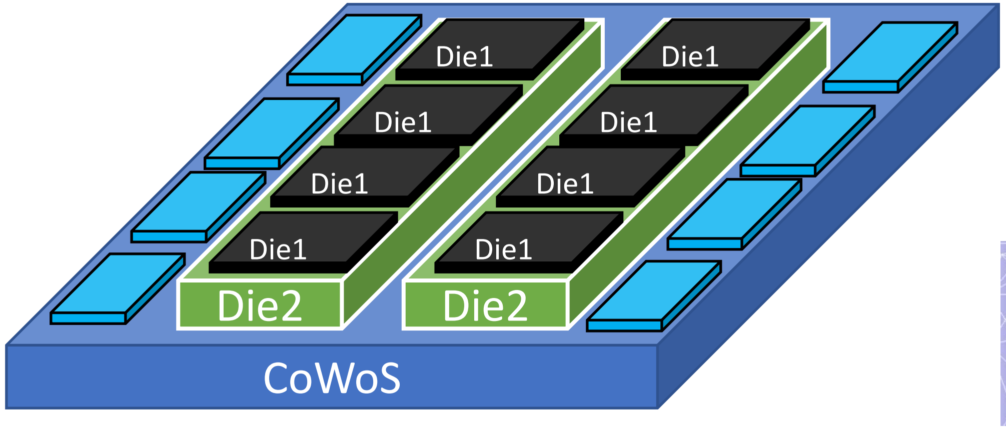
Selfheat FINFET, GAAFET, CFET, device to wire, wire to wire

Fatigue, Fracture, Vibration, Aging, Radiation…

High-Capacity Static Thermal Flow Much Needed for Large 3DIC

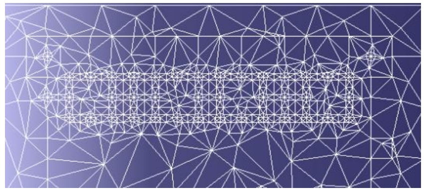
Driving applications: HPC / AI / 5G

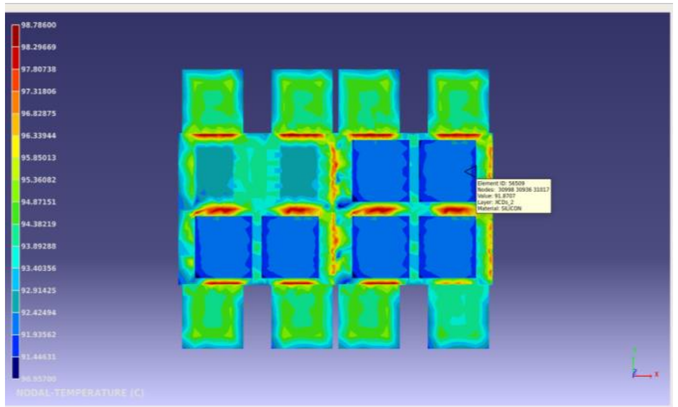
- ✓ Hierarchical thermal model stitching technique to assembly the thermal model to handle heterogenous 3D-IC system
- ✓ Global model simulation of 100µm*100µm low-resolution meshing within 5 hours, followed by detailed model simulation of each die using **Intelligent Adaptive Meshing** **in 1.5 hours**
- ✓ 3D-IC junction Tmax optimization with HTC applied on the package surface and heat spreader components included.



3D-IC system with GPU/CPU/HBM/logic dies
assembled on a 50mm*50mm CoWoS

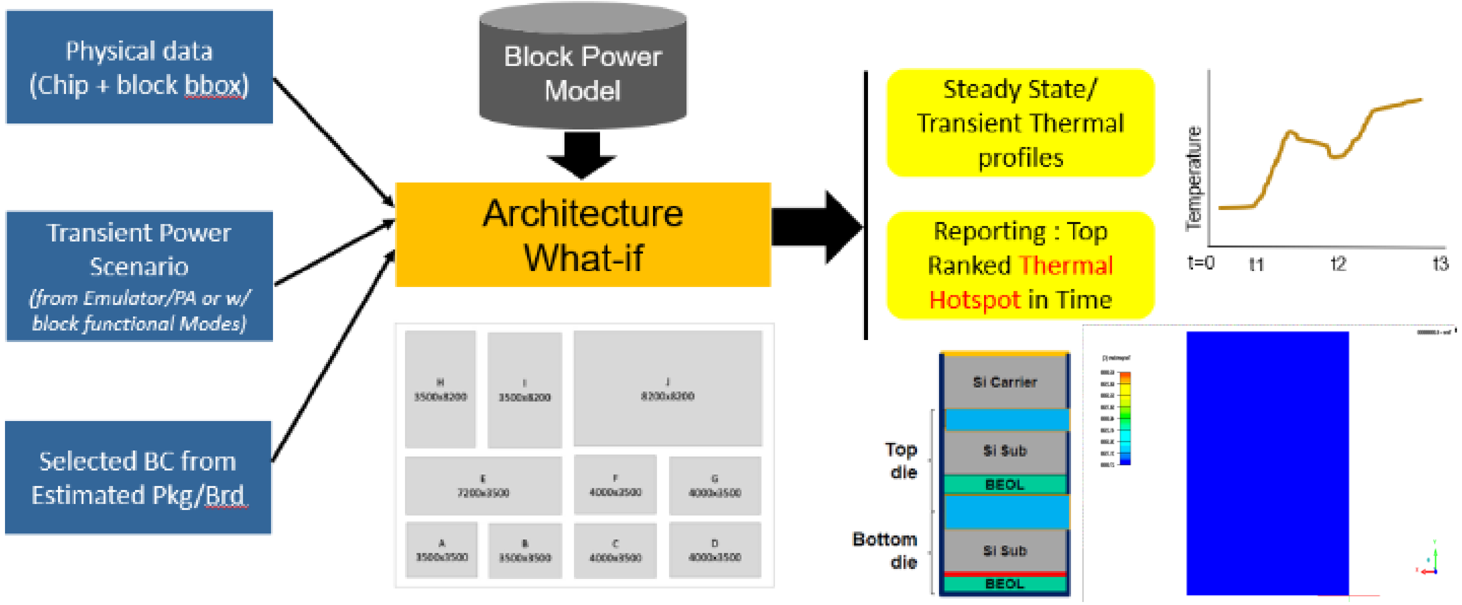
Intelligent Adaptative meshing
to reduce
total mesh count without
accuracy loss





Thermal result for large 3DIC

Fast Static/Transient Thermal Analysis



Physical data (Chip + block bbox)

Transient Power Scenario *(from Emulator/PA or w/ block functional Modes)*

Selected BC from Estimated Pkg/Brd

Block Power Model

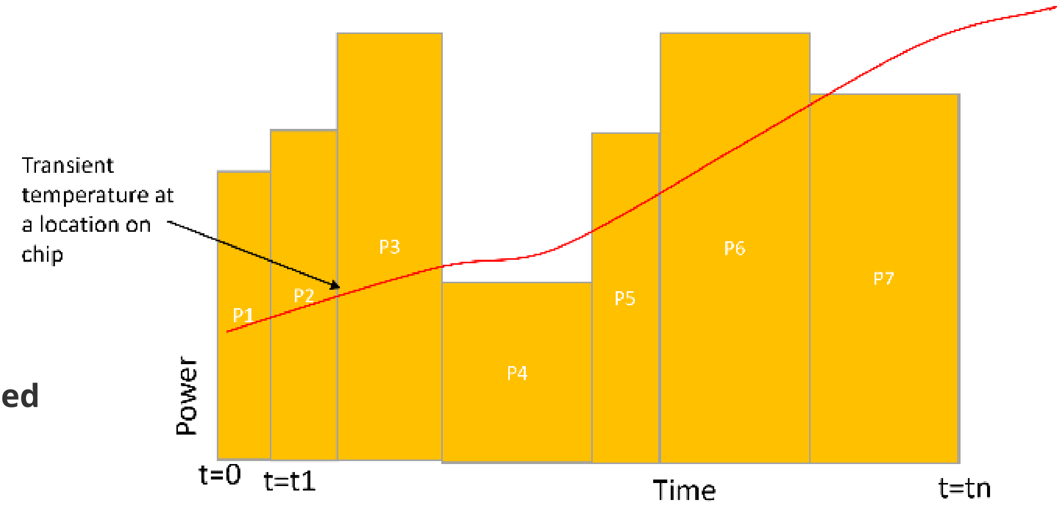
Architecture What-if

Steady State/ Transient Thermal profiles

Reporting : Top Ranked Thermal Hotspot in Time

- Performance and reliability degradation
  - Aging, EM, IR drops, stress, switching speed, etc.
- Fine grained thermal analysis on large 3DIC designs not possible using purely traditional FEA/CFD based approaches
- Long sequences of transient power need to be simulated to accurately predict how thermal hotspots change with time

Architecture level fast static/transient thermal analysis for various optimizations are required. (i.e. power/DvD/thermal/stress/test/sensor place)

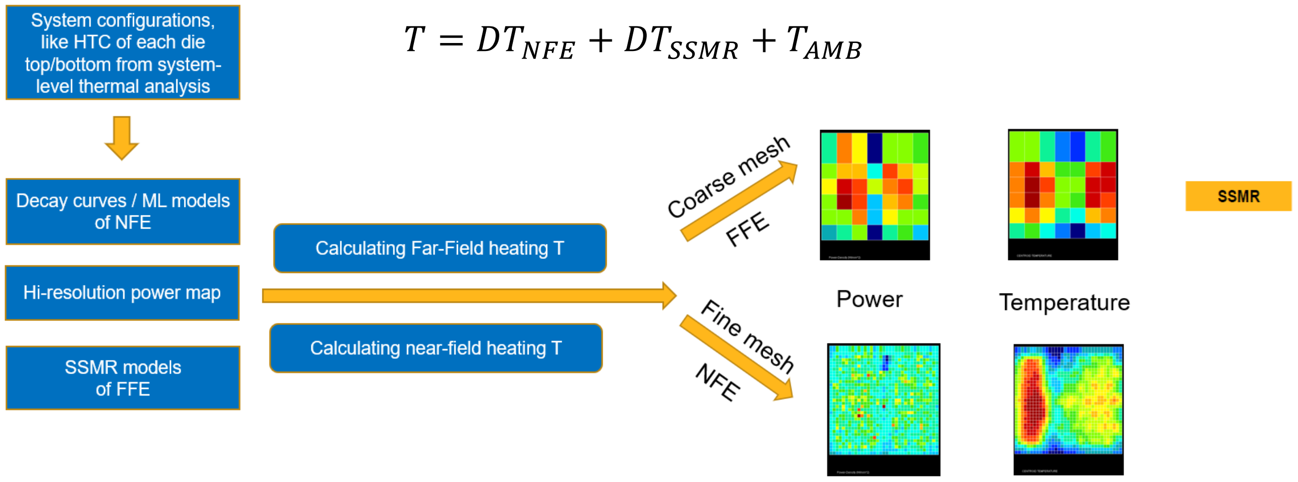


Transient temperature at a location on chip

"**Emerging Challenges on Thermal Modeling and Simulation for Advanced 3DIC Systems", N. Chang, Keynote, REPP, 2022**

ML-Augmented Static Thermal Solver for ML-based Hotspots Detection

$$T = DT_{NFE} + DT_{SSMR} + T_{AMB}$$



System configurations, like HTC of each die top/bottom from system-level thermal analysis

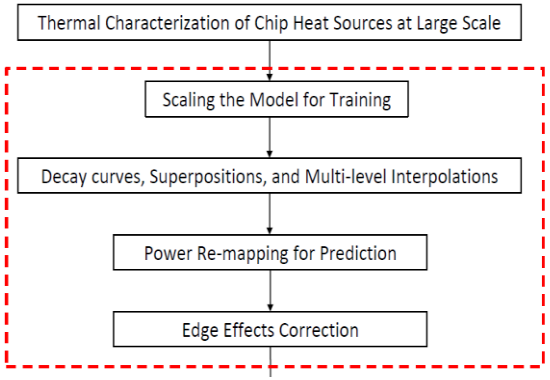
Decay curves / ML models of NFE

Hi-resolution power map

SSMR models of FFE

Calculating Far-Field heating T

Calculating near-field heating T



Thermal Characterization of Chip Heat Sources at Large Scale

Scaling the Model for Training

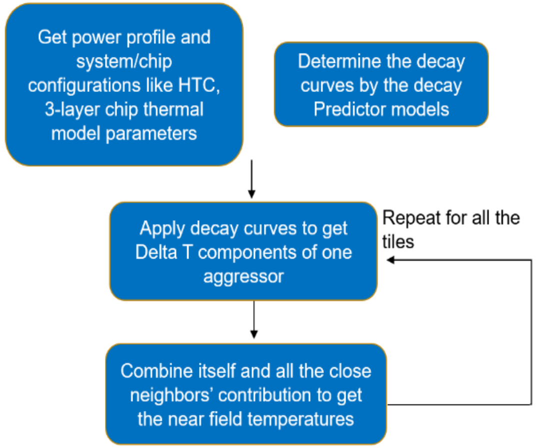
Decay curves, Superpositions, and Multi-level Interpolations

Power Re-mapping for Prediction

Edge Effects Correction

SSMR – Superposition and Scaling with Multi-Dimensional Interpolation and Remapping Based Scheme

Inferencing using the Decay models



Get power profile and system/chip configurations like HTC, 3-layer chip thermal model parameters

Determine the decay curves by the decay Predictor models

Apply decay curves to get Delta T components of one aggressor

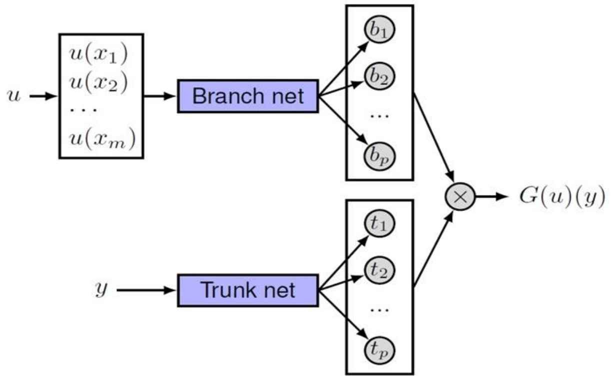
Combine itself and all the close neighbors' contribution to get the near field temperatures

Repeat for all the tiles

Two decay curve approaches in the flow:

- Characterize the decay curves in real-time at different locations. SSMR can be generated in real-time as well based on 3-layer die model.
- Use pre-trained decay ML models. The decay ML models will include both the nominal decay predictor and the decay dependency on locations and local thermal conductivity.
- With orders of magnitude faster than FEA/CFD solvers in a distributed computing framework based on SeaScape

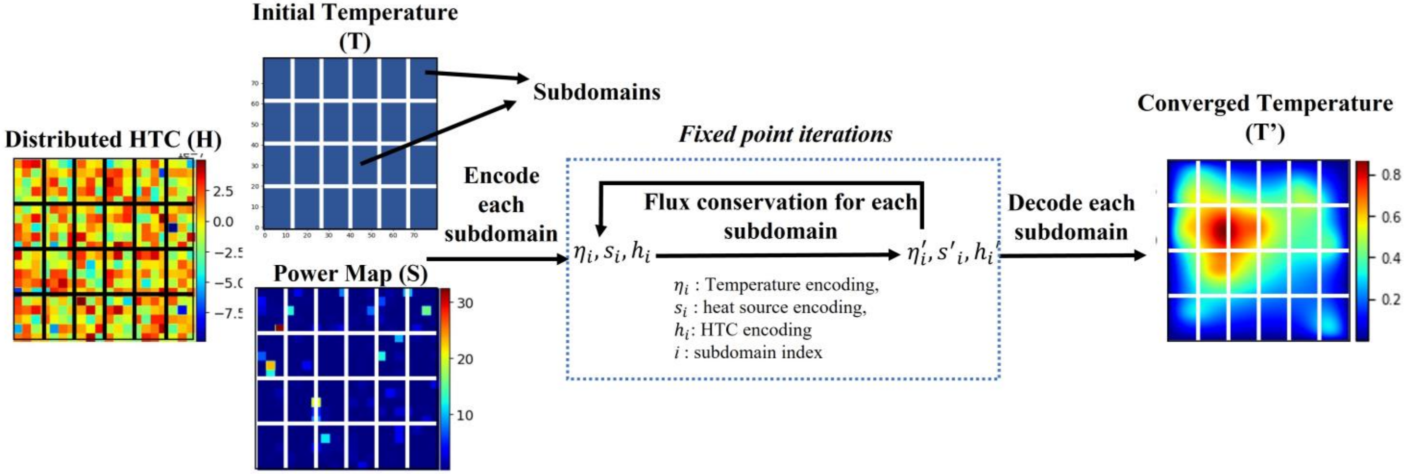
DeepONet network structure for pre-trained NFE model



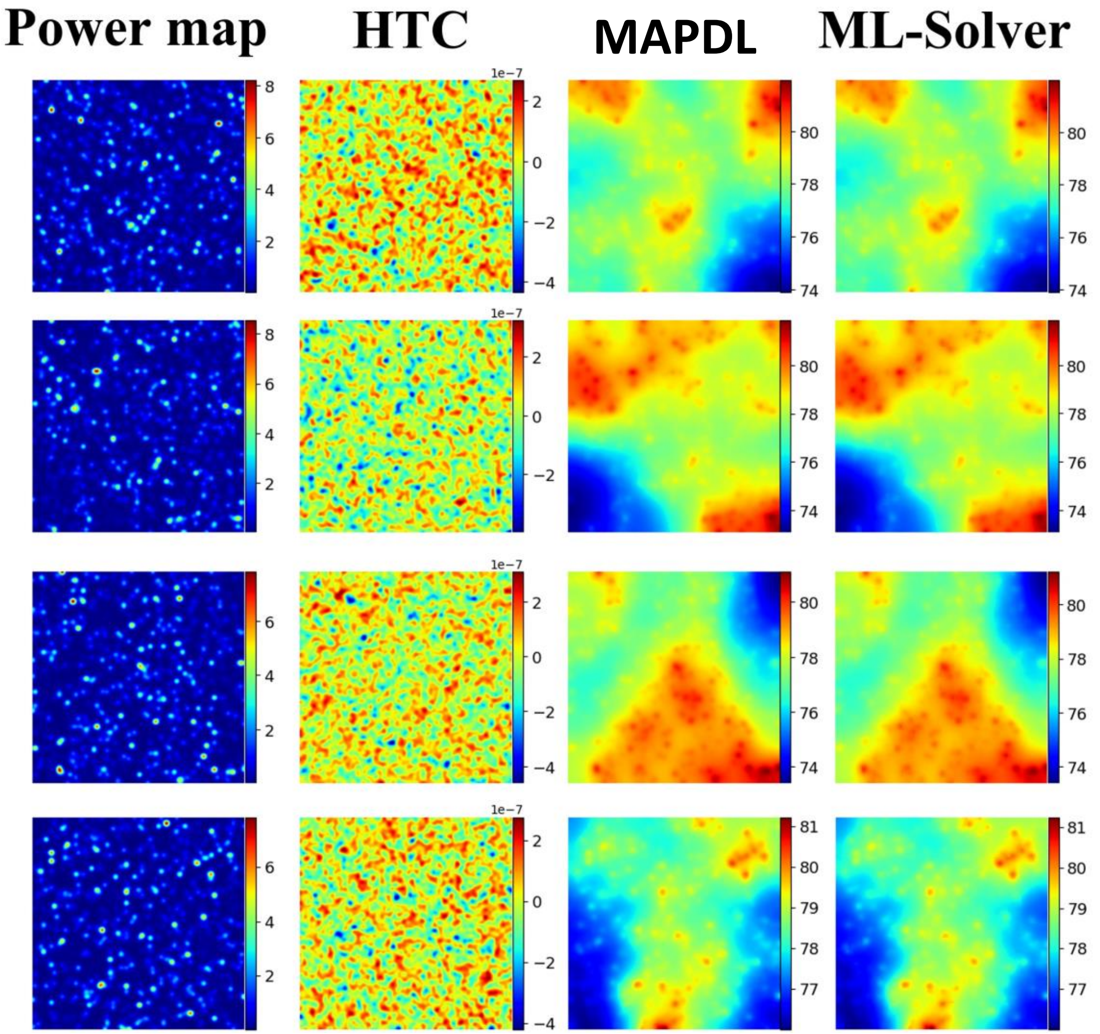
Input feature (unit)
Power (mW)
Effective HTC (mW/um^2*K)
Die size (um)
Die 3-layer model (um)
Thermal conductivity (mW/um*K)
Tile size (um)

Machine-learning based Static Thermal Solver with Distributed HTC

- Developed a novel Machine-Learning based Thermal solver to accurately predict chip temperatures for arbitrary power maps and distributed HTC patterns.
- The ML-Solver is inspired from keys ideas of traditional Ansys solvers. It iteratively solves for temperature on discrete subdomains given the power map, HTC and initial temperature. Flux conservation in each iteration is established using pre-trained ML models
- The ML-Solver is about 100x faster than current solvers and accurately predicts high-fidelity temperature maps on the chip.



Ranade, R., Haiyang, H., Pathak, J., Kumar, A., Wen, J. & Chang, N. (2022). A Thermal Machine Learning Solver for Chip Simulations. *4th ACM/IEEE Workshop on Machine Learning for CAD*



Optimization of Mobile Pkg Material Calibration for Thermal/Stress Integrity

IEEE ELECTRONICS PACKAGING SOCIETY
ECTC
The 2024 IEEE 74th Electronic Components and Technology Conference

As-is process/Challenges

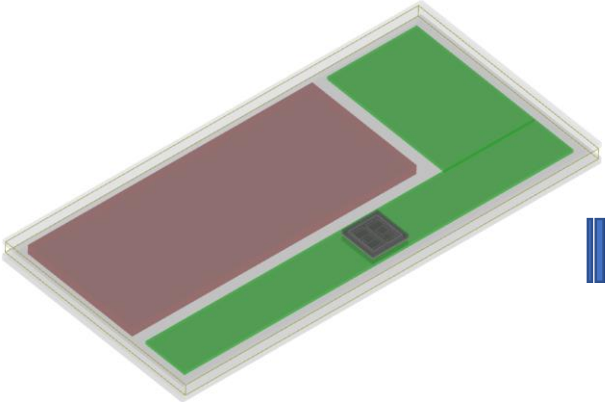
- Sensitivity analysis of thermal material properties of mobile AP
- Fast and Accurate equivalent virtual thermal testing model → Simple Model
- Trial & Error approach for fine tuning material → Expensive!
- Too many trials (1000+) need to be performed for 10+ parameters
- Challenges:
    - Significant manual effort for 1000+ trials
    - Accurate simple model for transient thermal analysis
    - Reduced Dependency on package type

Ansys Value Stream

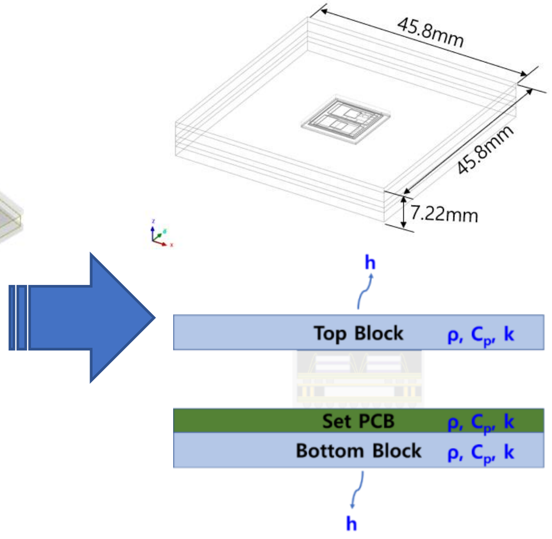
- Robust workflow integration and optimization with optiSLang-AEDT Icepak
- Reduced input BC conditions and material properties (h,K,CP and Den)
- Sensitivity analysis with thermal material parameter of components.

Outcome

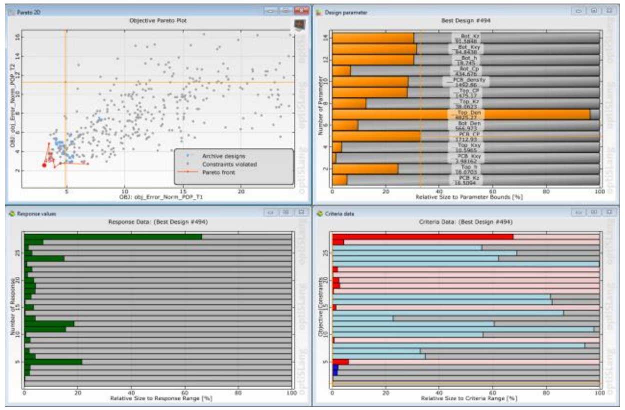
- Extract optimized equivalent properties of Simple model that is well matched with reference data
- Automatic DOE reduction to reduce the overall time for optimization.
- Reduced time for optimization and increased accuracy
    - 2~4 Weeks → 4~5 Days

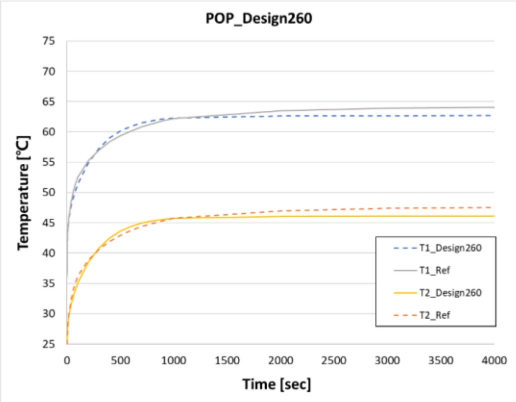


Full set model of smartphone



Simple model with equivalent thermal material property





Ansys

"Thermal Model Simplification of Mobile Device with Adaptive Metalmodel of Optimal Prognosis (AMOP)", V. Krishna, et al., iTherm, 2022